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Fabrication of Silicon-based Nano-structures and Their Scaling Effects on Mechanical and Electrical Properties

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Fabrication of Silicon-based Nano-structures and Their Scaling Effects on Mechanical and Electrical Properties

by

Bin Li, B.E.; M.E.

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

December 2007

Dedication

To my family

Acknowledgements

I would like to thank many people for helping me during the past six years. I would especially like to thank my advisor, Prof. Paul Ho, for his continuous support and advice throughout my doctoral work. I am also very grateful for having an exceptional doctoral committee and wish to thank Prof. Li Shi, Prof. Rui Huang, Prof. Lew Rabenberg, Prof. Xiaojing Zhang, and Dr. Michael W. Cresswell for their support and encouragement. I specially thank Dr. Jang-Hi Im, Dr. Ryan Scott Smith, and Dr. Michael W. Cresswell for proofreading my dissertation and for their valuable suggestions.

I also want to take this opportunity to thank my colleagues and friends in the Laboratory for Interconnect and Packaging for their advice and discussions about my research. I am also thankful to Ms. Jo Ann Smith for her help. I would like to thank my Chinese friends on the J.J. Pickle research campus for their warm friendship.

Finally, I'd like to thank my family. I'm grateful to my parents and my wife for their continuous encouragement and patience. I am also thankful to my parents-in-law for helping me accomplish this work. I'm especially grateful to my wife Feng for her support, dedication and endless love.

Fabrication of Silicon-based Nano-structures and Their Scaling Effects on Mechanical and Electrical Properties

Publication No._____

Bin Li, Ph.D.

The University of Texas at Austin, 2007

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Silicon-based nanostructures are essential building blocks for nanoelectronic devices and nano-electromechanical systems (NEMS), and their mechanical and electrical properties play an important role in controlling the functionality and reliability of the nano-devices. The objective of this dissertation is twofold: The first is to investigate the mechanical properties of silicon nanolines (SiNLs) with feature size scaled into the tens of nanometer level. And the second is to study the electron transport in nickel silicide formed on the SiNLs. For the first study, a fabrication process was developed to form nanoscale Si lines using an anisotropic wet etching technique. The SiNLs possessed straight and nearly atomically flat sidewalls, almost perfectly rectangular cross sections and highly uniform linewidth at the nanometer scale.

To characterize mechanical properties, an atomic force microscope (AFM) based nanoindentation system was employed to investigate three sets of silicon nanolines. The SiNLs had the linewidth ranging from 24 nm to 90 nm, and the aspect ratio

(Height/linewidth) from 7 to 18. During indentation, a buckling instability was observed at a critical load, followed by a displacement burst without a load increase, then a fully recoverable deformation upon unloading. For experiments with larger indentation displacements, irrecoverable indentation displacements were observed due to fracture of Si nanolines, with the strain to failure estimated to be from 3.8% to 9.7%. These observations indicated that the buckling behavior of SiNLs depended on the combined effects of load, line geometry, and the friction at contact. This study demonstrated a valuable approach to fabrication of well-defined Si nanoline structures and the application of the nanoindentation method for investigation of their mechanical properties at the nanoscale.

For the study of electron transport, a set of nickel monosilicde (NiSi) nanolines with feature size down to 15 nm was fabricated. The linewidth effect on nickel silicide formation has been studied using high-resolution transmission electron microscopy (HRTEM) for microstructural analysis. Four point probe electrical measurements showed that the residual resistivity of the NiSi lines at cryogenic temperature increased with decreasing line width, indicating effect of increased electron sidewall scattering with decreased line width. A mean free path for electron transport at room temperature of 5 nm was deduced, which suggests that nickel silicide can be used without degradation of device performance in nanoscale electronics.

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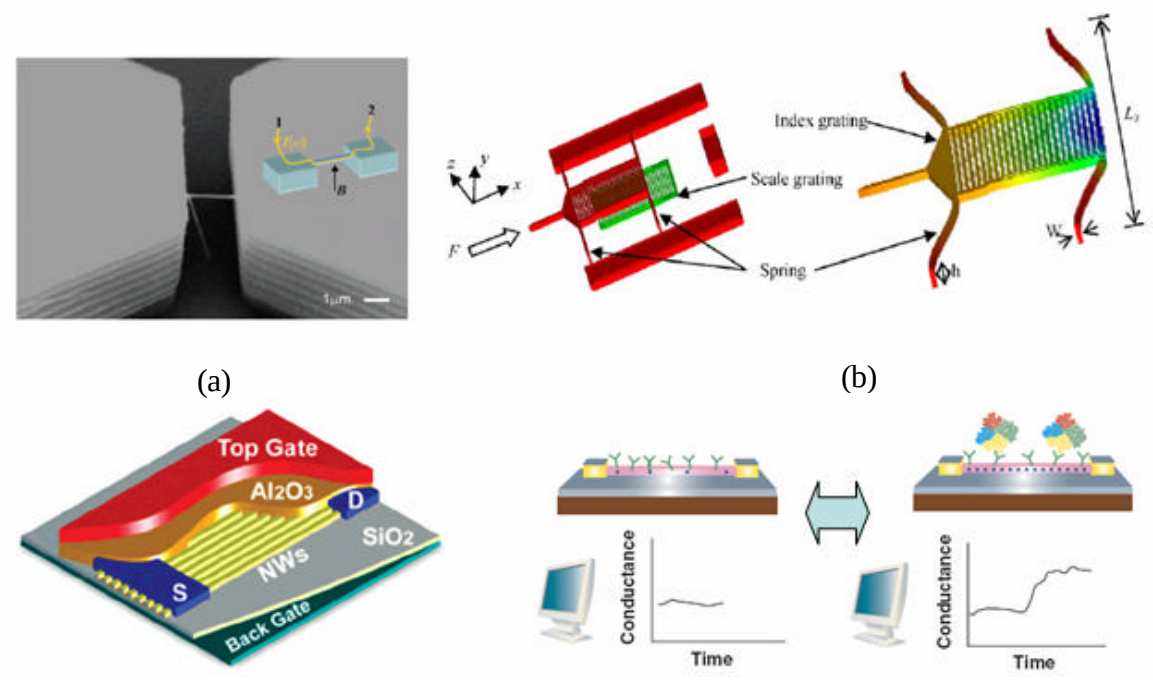
Chapter 1 Introduction

As the scaling of device dimensions continues, fabrication of nanoscale structures and the characterization of their mechanical and electrical properties pose significant challenges for future development of ultra large-scale integrated (ULSI) and gigascale integrated (GSI) circuits [1,2,3]. In particular, silicon-based nanostructures can serve as essential building blocks for nanoelectronic devices and nano-electromechanical systems (NEMS) [4,5,6,7]. For example, nanoscale silicon nanowires (SiNWs) were used as high quality oscillator for resonant sensing in nanomechanical systems [8,9]. Silicon nano-beams can be used as nano-gratings for high-precision optical measurement of displacement [10,11]. As an important component in nano-devices, silicon-based nano-structures were employed to form nano-scale electronic field-effect-transistors (FETs) [7,12,13], or ultra-sensitive sensors for detecting biomedical species or single electron spin [5,14], etc. Figure 1.1 shows some applications of silicon-based nanowires in NEMS and nanoelectronic devices.

During operation, the nano-structures are subjected to external forces or electrical current, which enable the function of devices. Hence, the mechanical and electrical properties of the nanostructures play an important role in controlling the functionality and reliability of the nano-devices. Fundamental knowledge of the physical properties, *e.g.* elastic modulus, fracture strength or resistivity, particularly, dimension scaling effect on these properties [15,16,17,18], is essential for improving the design and reliability of nano-devices. Thus, the investigation of the material properties of silicon-based structures

at the nano-metric scale is significant both for scientific understanding and practical applications.



(a) (b)

(c) (d)

Figure 1.1 Silicon-based nanowires in NEMS or nanoelectronic devices. (a) Scanning electron microscopy (SEM) image of silicon nanowire grown in a microtrench [9]. Inset: illustration of magnetomotive transduction of a SiNW [9]. (b) Nano-gratings in optical-encoder sensor for high-precision measurement of displacement [10]. (c) Schematic drawing of a SiNW FET, with the electrodes labeled [13]. (d) Schematic of a nanowire device as a sensor with antibody receptors, and the binding of proteins yields an increase in the conductance [5].

Fabrication and the corresponding characterization metrologies of the silicon-based nano-structures are still of great challenge, particularly for a feature size in the range of tens of nanometer. In this dissertation, the scaling effect on physical properties of silicon-based nano-structures will be investigated. The study includes three parts: fabrication process developed for formation of well-controlled silicon-based nano-

structures, characterization of mechanical properties of silicon nanolines (SiNLs) and electrical study of nickel silicide (NiSi) nanolines.

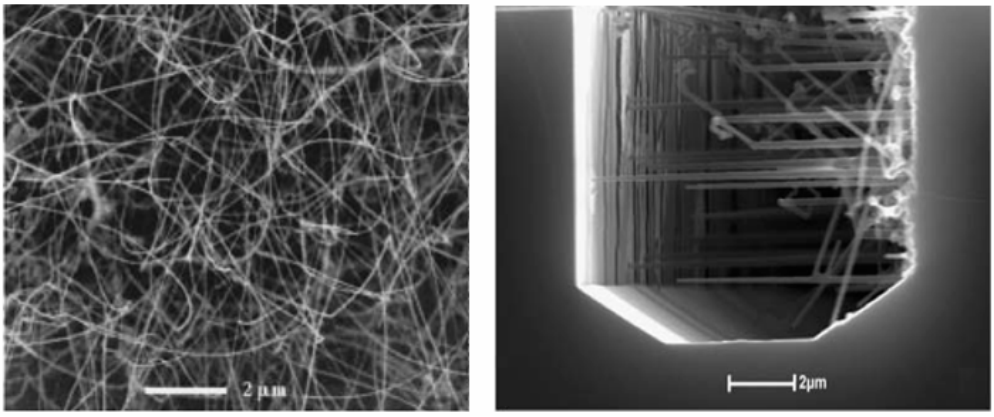
Chapter 1 will discuss the challenges of fabricating and characterizing nano-structures, objectives and literature surveys on mechanical and electrical characterizations on nano-structures, respectively. The chapter concludes with an overview of the dissertation.

1.1 Challenges of fabrication and characterization of nano-structures

In order to investigate mechanical or electrical properties of nano-structures, it is necessary to fabricate good quality nanostructures with controlled microstructure and geometry [19,20,21]. Fabrication of well-controlled silicon-based nanostructures is a big challenge. Generally there are two approaches for creating small scale nano-structures: bottom-up and top-down approaches.

The first approach employs a bottom-up synthesis method, in which single crystalline nano-structures are formed through two fundamental steps: nucleation and growth, by well-defined chemical or physical synthesis processes. For example, in the past decade, the vapor-liquid-solid (VLS) process [22,23,24] and metal-catalyzed chemical vapor deposition (MCCVD) [19,25] were successfully developed to grow single crystalline silicon nanowires with diameter around 10-100 nm. Figure 1.2 shows two scanning electron microscope (SEM) images of SiNWs grown by the bottom-up approaches. The feature size of the obtained nanowires could be as small as 10 nm, which is not restricted by the resolution of conventional lithography tools. However, it is difficult to control precisely on the nanowire dimensions, and to form proper test

structures during the fabrication. Moreover, the placement of the nanowires for measurements can be very challenging.

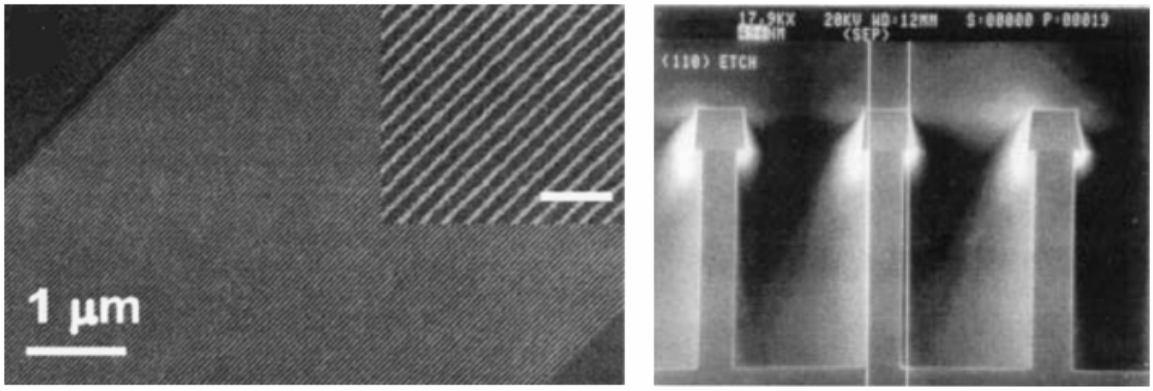


(a) (b)

Figure 1.2 (a) Plan view SEM image of SiNWs formed by VLS process [22]. (b) cross-sectional SEM image of lateral epitaxial SiNWs grown between microtrench by MCCVD process [25].

In the top-down approach, nano-structures are first patterned and then transferred into bulk or film materials. Typically the pattern is formed by nano-lithography processes, *e.g.* E-beam lithography (EBL) [26], superlattice nanowire pattern transfer (SNAP) [27], nanoimprinting (NIL) [28], etc. The pattern is then transferred to the substrate by wet etching or dry etching processes [3, 29]. Sub-40 nm silicon nano-structures can be successfully formed by pattern transfer into a Si substrate by reactive ion etching (RIE) processes. But the quality of the small structures is subjected to plasma damage. This can significantly affect the sidewall roughness or the uniformity of nanostructures, and the electrical performance of nano-devices [20, 30]. Another pattern transfer technique is anisotropic wet etching (AWE). It has been used to fabricate silicon nanostructures, having vertical and smooth sidewalls without ion-bombardment and plasma induced

defects [31, 32]. However, the feature size was limited by two factors: lithography process (*e.g.* optical lithography or field enhanced anodization technique), and the stringent requirement for orientation alignment under small dimensions in AWE [33]. Figure 1.3 shows two SEM images. In Figure 1.3(a) it is a set of 12 nm wide lines fabricated by RIE, where line edge roughness was due to plasma damage. In Figure 1.3(b) some silicon wide lines were made by AWE, showing vertical and smooth sidewalls.



(a) (b)

Figure 1.3 (a) 12 nm wide SiNWs generated by SNAP process. Pattern was transferred into silicon using CF_4+O_2 plasma etching, showing line roughness due to ion bombardment. The scale bar in the inset is 150 nm [20]. (b) SEM image of feature cross-sections of silicon lines after KOH wet etching on (110) Si wafer. The silicon nitride hard-mask caps had not been removed [34].

One objective of this study is to develop a new fabrication process to further reduce the feature dimensions and to form well-controlled nano-structures. This process is based on a combination of high resolution of EBL with high quality pattern transfer by AWE, which is used to obtain vertical and smooth single-crystal SiNLs on (110) orientated Si. The SiNLs fabricated have potential applications for nanograting-based sensors [10] and interconnects [25], and are also well-suited for quantitative studies of

mechanical or electrical properties of silicon-based structures at nanometer scale. Thus they were used in the measurements of this study.

Besides fabrication, characterization of nano-structures is also challenging [35]. First of all, handling of extremely small structures is difficult. Due to their small dimension, it can be very challenging to manipulate or position nanoscale specimens without inducing any damage [36]. Secondly, suitable metrology tools for quantitative measurements of the properties are of great importance. SEM or transmission electron microscope (TEM) are required for debugging and monitoring fabrication processes, or performing micro-structural analysis [37]. Meanwhile, high resolution transducer for measurement also plays an important role. For example, the force required to break a silicon nano-beam could be in nano-Newton range [19]. Precision of the experiment control in such a small range becomes very difficult.

In the next two sections, a mechanical analysis of silicon nano-structures and an electrical study of nano-scale conductors are reviewed based on literature surveys. Subsequently, the objectives of mechanical and electrical characterization on the silicon-based nano-structures are presented.

1.2 Mechanical characterization of silicon nano-structures

The scaling effect on mechanical properties is readily observed and is generally attributed to a change in the properties due to the small dimension of internal structure or in the overall sample size. Well-known examples are the improvement of the yield strength of metallic alloys through refinement of the grain size [38,39] and fine whiskers [40]. For nano-structures, with dimension approaching micro- or nano-meter ranges, the

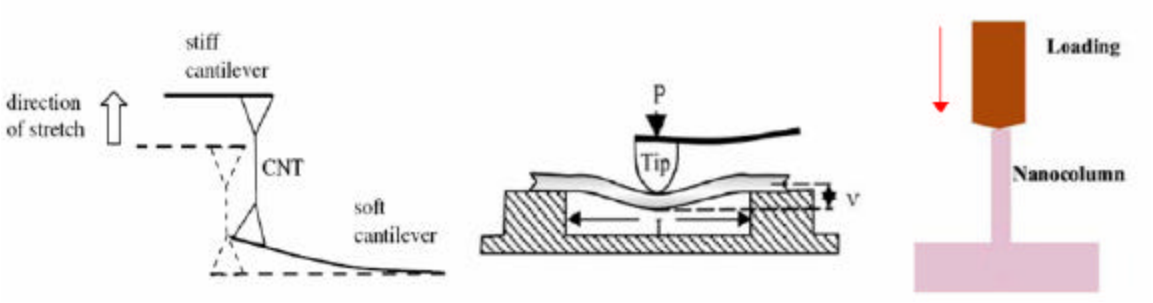
sample size is expected to become an important factoring controlling their mechanical strength. Previously, single-crystal silicon (Si) beams with widths from 200 nm to 800 nm have been fabricated by field-enhanced anodization using an atomic force microscope (AFM) [41,42,43]. Mechanical characterization of these Si beams by AFM bending tests showed a strong size effect on bending strength, which is defined to be the maximum tensile stress in a specimen bent up to fracture, but no size effect on Young's modulus was observed[41,42]. The reported bending strength was in the range of 11 GPa to 18 GPa, significantly higher than the average strengths for microscale Si beams (4 GPa) [44] and millimeter scale Si beams (around 500 MPa) [41]. It appears that the strength of nanoscale single-crystal Si beams can soon achieve the theoretical fracture strength of Si, predicted to be 22 GPa under tension with a critical strain of 17% [45]. Recently, MCCVD had been developed to grow high-quality single crystal SiNWs with diameters ranging from 50 to 350 nm. Both single and double clamped SiNWs were characterized by AFM bending tests [15,19,46]. Again, no size effect was found for the Young's modulus [15, 46]. For SiNWs with diameters between 90 nm and 200 nm, Hoffmann et al. [15] reported an average strength around 12 GPa, while Tabib-Azar et al. [19] reported much lower strengths in the range of 210 MPa to 830 MPa for longer SiNWs (10 μm vs 2 μm), possibly due to process-induced defects and friction at the contact between the AFM tip and the SiNWs. No data has been reported so far for the strength of SiNWs with feature size less than 90 nm.

In addition to the AFM bending tests, other methods for nanoscale mechanical characterization have been developed, such as mechanical resonance [47,48], nano-

tensile [36,49], and nanoindentation tests [50,51,52,53]. Figure 1.4 shows schematic diagrams of nano-tensile testing, AFM bending test and nanoindentation test of nano-structures. In general, characterization of mechanical properties at the nanoscale level requires precise manipulation of nanoscale specimens and high-resolution force/displacement measurements. The resonance method is limited to the measurement of elastic properties only. Nano-tensile test was used to measure elastic modulus and fracture strength of carbon nanotubes (CNTs) [36], which is inherently difficult due to problems in obtaining proper CNT gripping and specimen alignment. For AFM bending test, it was widely used for measurements of mechanical behavior of SiNWs. However, the interpretation of the results is complicated, because of the uncertainties in reproducing the nanowire bending behavior, due to slipping or swinging of wires, as well as the ambiguity of defining boundary conditions at the support ends [41,54,55]. The nanoindentation technique is well established for the measurement of elastic modulus, hardness, and fracture toughness of both bulk and thin film materials [56,57]. The precision in both force and displacement measurements, together with easy sample preparation, have led to recent applications of this technique for the mechanical characterization of various nanomaterials including nanotubes [50], nanowires [51], nanobelts [58], and nanoparticles [59]. However, interpretation of the nanoindentation results is nontrivial and often requires sophisticated modeling [60,61].

In this study, the nanoindentation technique along with numerical simulations by a finite element methods (FEM) are employed to characterize the mechanical properties of the SiNLs, yielding elastic modulus, strain to fracture of SiNLs, and friction

coefficient at the contact with the indenter tip. This also demonstrates a novel nanomechanical testing method of patterned nanostructures.



(a) (b) (c)

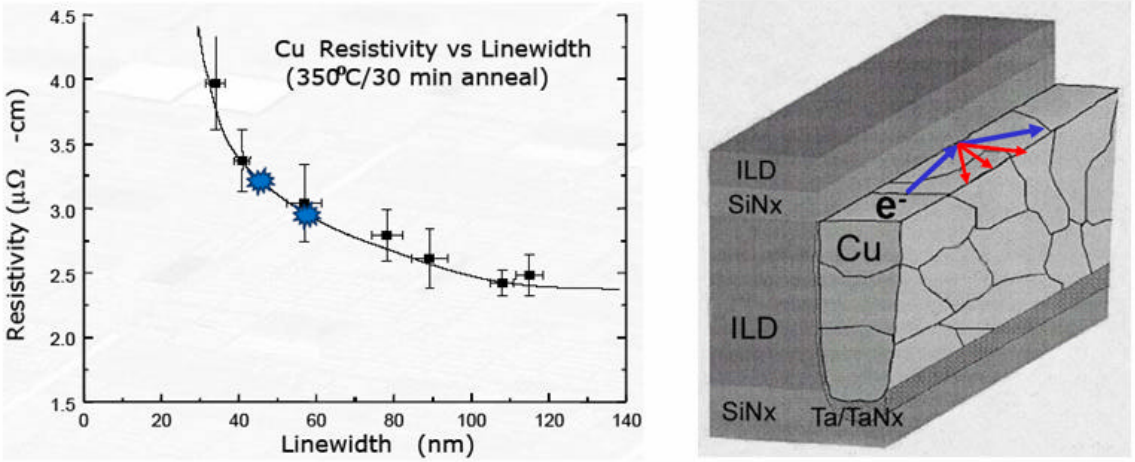
Figure 1.4 (a) Schematic diagram of using AFM cantilevers to perform Nanotensile test on CNT [35]. (b) Schematic diagram of an AFM bending test on a SiNW [62]. (c) Diagram of Nano indentation on a nanocolumn [53].

1.3 Electrical transport study on nano-conductors

As devices continue to scale down from the current 90 nm node to below 45 nm, new limitations of the functionality of copper interconnects have to be considered [63,64]. With decreasing linewidth, disproportionate increases in copper-interconnect resistance occur. This is partly due to barrier-metal coating that is used to inhibit copper migration into the interlayer dielectric. Since the thickness of the barrier-metal coating does not scale with the linewidth of the copper-interconnect feature, the fraction of the cross-sectional area consumed by the high-resistivity barrier coating, as a fraction of the total cross section, increases [65]. As the linewidth decreases below 100 nm, the resistance of the copper core itself increases due to increasing grain-boundary and sidewall-surface scattering of electrons [66,67]. Even if the contribution from the barrier-metal coating to the total interconnect resistance is mitigated by new and improved fabrication techniques, increased surface scattering is expected to elevate effective resistivity to levels that may

significantly exceed the 2.2 μO-cm target set in the ITRS roadmap [21,68]. Figure 1.5(a) shows copper resistivity vs. line width in copper interconnects, indicating an impact of critical dimension (CD) on copper resistivity.

Study of the scaling effect on effective electrical resistivity of metal conductor has stimulated significant interest. Recently as the external dimension or grain size of the nanostructure is comparable to the electron mean free path (40 nm for Cu at room temperature), increase of the total resistivity is mainly attributed to the enhanced scattering of electrons from the surfaces. The resistivity increases can be accounted for based on the Fuchs-Sonderheimer (FS) theory [69,70], and from the contribution of grain boundaries as described by Mayadas and Shatzkes [71]. Figure 1.5(b) shows a schematic diagram for an electron scattered at interfaces and grain boundaries in a copper interconnect.



(a) (b)

Figure 1.5 Impact of critical dimension on resistivity of copper interconnects. (a) Copper resistivity vs. line width [30]. (b) Schematic diagram electron scattered at interfaces and grain boundaries in a copper interconnect [21].

However, a proper analysis of the measured data, which is acquired in studies of surface and grain boundary scattering, is usually difficult due to the difficulty of microstructure control in an ultra-small volume [21,30]. For ultra-fine copper lines, the problem can be traced to the difficulty of controlling the fabrication of copper damascene lines of sub-100 nm dimensions. Key fabrication steps include reactive ion etching of low-k dielectrics, deposition of ultra-fine barriers, electroplating of copper, and chemical-mechanical polishing (CMP). These processes are important in defining the copper grain structure as well as the defect level of the line surface and its interface, but they are very difficult to control. Another example is silicide formation and its electrical properties in nano-scale dimension. The Self-aligned silicide (SALICIDE) is widely used in conventional silicon manufacturing. Low-resistivity nickel monosilicide (NiSi) is of considerable interest as a contact and interconnect material for 45 nm node technology and beyond, due to its low resistivity, low silicon consumption and low formation temperature window [72,73,74,75]. It was found that NiSi formation was subjected to a linewidth effect with scaling of CD below 100 nm, resulting in a change of electrical performance [17, 76]. Thus, there is an inherent need to develop the scientific and engineering foundations to understand the microstructure and electrical characteristics of ultra-narrow conductors.

In response to this challenge, mono-crystalline NiSi fine lines, which had nano-scale dimensions and highly controlled surface microstructures, were formed by controlling the fabrication conditions. Silicide microstructural analysis and the resistivity measurements on a number of samples were performed.

1.4 Overview of the dissertation

The purpose of this dissertation is to investigate mechanical and electrical properties of silicon-based structures at the nanometer scale. The main part of this dissertation is divided into 4 chapters. The fabrication process will be presented in Chapter 2. Mechanical measurement results will be discussed in Chapter 3 and Chapter 4, respectively. Electrical test results will be presented in Chapter 5.

In Chapter 2, the process development for the formation of single-crystal Si nanolines will be presented. Instead of using nanoimprinting and reactive ion etching (RIE) processes for pattern formation, a process combining electron-beam lithography for definition of the feature size, with anisotropic wet etching for high quality pattern transfer, was developed. The process details, which include nanolithography process control, methods to perform orientation alignment in wet etching, etc, will be discussed.

Chapter 3 and Chapter 4 will present mechanical test results on the fabricated SiNLs. An AFM based nanoindentation system was used to measure the mechanical response of these SiNLs, and a FEM model was developed to simulate the indentation process and to extract material properties, including elastic modulus and strain to fracture. Buckling instability was observed at a critical load, where the friction at the contact between the indenter and SiNLs was found to play an important role in controlling their buckling behavior. Chapter 3 focuses on setup of the characterization and analysis method to extract mechanical properties of SiNLs using nanoindentation. In Chapter 4, the method developed was applied to measure SiNLs as a function of nanoline geometry, extending to a feature size as small as 24 nm and an aspect ratio as high as 16. The

experimental data of indentation as well as the corresponding FEM simulation will be presented.

The electrical study on fine nickel silicide lines will be presented in Chapter 5. The chapter begins with a microstructure analysis of silicide formation under different processing conditions, followed by electrical resistivity measurement on silicide nanolines with feature size down to 25 nm. The Fuchs-Sonderheimer theory was applied to the analysis of resistance results at room temperature, and the electron sidewall scattering effect was investigated at cryogenic temperatures. The details of analysis will be discussed in this chapter.

Finally, Chapter 6 presents a summary of the dissertation and some suggestions for future work.

Chapter 2 Fabrication of Silicon Nano-structures

In chapter 2, the focus is on the process development for fabrication of silicon nano-structures. In the fabrication process, lithography of patterns and the subsequent pattern transfer are the two key fabrication steps. Patterns are first created by lithography tools in a resist layer, *i.e.* nanoimprinting lithography (NIL) [77,78] or EBL [79], which determine feature size of nano-structures. Then patterns are transferred to the substrate using a selective etching process, *i.e.* reactive ion etching (RIE) [80] or AWE process [31], which is directly related to the quality of the formed nano-structures. In this chapter, two lithography techniques, NIL and EBL, are first discussed regarding the quality of resist patterns and the process yield. Related to the pattern transfer step, comparison among RIE, lift-off and AWE, will be made regarding the etching quality of the silicon nano-structures obtained. In the third section, a process developed to improve the quality of fabricated nano-structures, is illustrated by assembling EBL and AWE, in forming silicon nano-structures with vertical and flat sidewalls with feature size down to ~25 nm. Finally, a summary of the fabrication process developed will be presented.

1.1 Lithography techniques

According to ITRS 2006 updates, the requirement for continuous miniaturization of ultra large scale integrated (ULSI) circuit devices will lead to the 22 nm node in 2010 [68]. Therefore, due to the processing and resolution of photolithography, it is necessary to develop new processes for the fabrication of nanostructures. E-beam lithography (EBL), which is a serial patterning approach and does not need a mask, has been used for

fabrication of sub-30 nm nano-structures [26]. Meanwhile, some low cost lithography methods, such as nanoimprinting [77], AFM based lithography [81], Step and Flash imprint lithography (SFIL) [82], etc, have been developed in the past two decades to fabricate nanostructures with feature size down to tens of nanometers. In the process development, NIL was first applied to make polymer patterns, and EBL was used for a better process control. The details of the investigation of these two techniques are in the following.

2.1.1 Nanoimprinting lithography (NIL)

NIL is a relatively straightforward, high throughput, and cost effective technique that has been developed by Chou *et al* for feature size as small as 20-30 nm [77, 83]. There are two basic steps in NIL, which are shown schematically in Figure 2.1. At first in the imprint step a mold with pattern on surface is impressed into a resist layer on top of substrate surface, followed by the withdrawal of the mold with a replicated pattern left in the resist film. The second step is the pattern transfer process by an RIE process, which removes the residual resist in the compressed area. This step is necessary to transfer the thickness contrast into the entire depth of the resist layer.

In the imprint step, the resist film needs to be treated properly, *i.e.* by thermal heating [77] or UV curing (82), to facilitate formation of the resist pattern. Figure 2.2 shows schematics of these two methods [28,78]. In the thermal imprinting process, the resist layer is heated up to reduce its viscosity, and then the mold is pressed into the resist to form the thickness contrast, which is shown in Figure 2.2(a). As an UV curing process, the step-and-flash imprint lithography (S-FIL) was developed by Willson *et al*, which

applies a transparent mold first pressing into a liquid resist, and then follows by a UV light curing to solidify the resist pattern. This process is summarized in Figure 2.2(b).

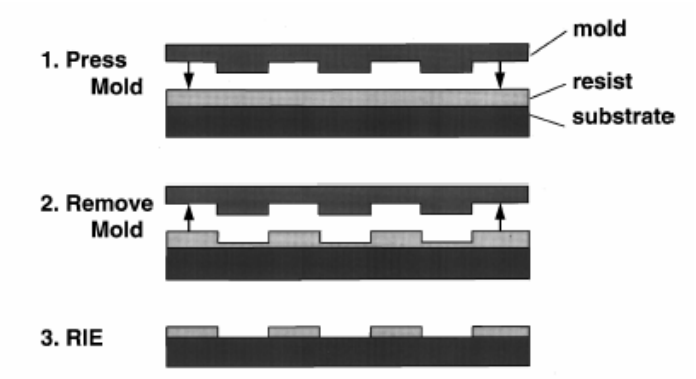
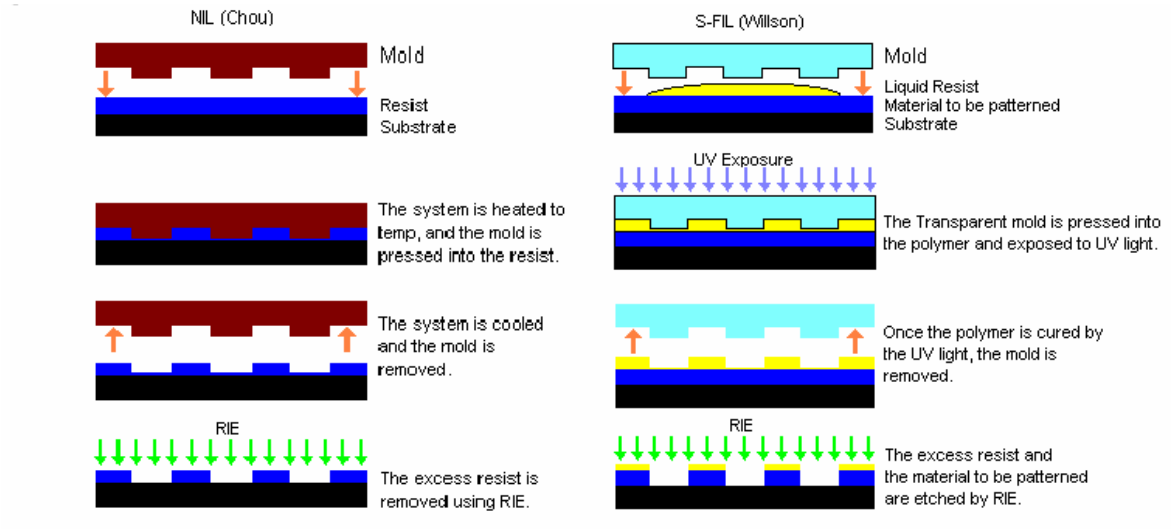


Figure 2.1 Schematic of NIL process. (1) imprinting using a mold into a resist layer; (2) mold removal and left pattern in resist, and (3) remove residual resist in the compression area using RIE [77].



(a) Thermal Imprinting (Chou) (b) S-FIL Imprinting (Willson)

Figure 2.2 Schematics of the two imprinting process. (a) Thermal imprinting developed by Chou *et al*; (2) Step and flash imprint lithography (S-FIL) developed by Willson *et al* [28].

It is apparent in both of the two processes, the resolution of the replicated pattern is determined by the feature size of the mold pattern. The quality of the replicated pattern is dependent on both the quality of the mold pattern and the performance of the imprinting process.

A. Superlattice nanowire pattern transfer

The fabrication of the mold is very critical to the imprinting process. One challenge of the application of NIL is the fabrication of the imprint mold with sub-20 nm feature size. Recently, Melosh *et al* developed a method of producing such imprint molds by selectively etching the AlGaAs layers of an AlGaAs/GaAs superlattice wafer, and transferring metal lines evaporated on the etched cross section surface of the superlattice on a planar substrate to produce high-density sub-20 nm wide nanowire arrays [27]. The method is named as superlattice nanowire pattern transfer (SNAP), which features with the idea of translating thin film growth thickness control into planar wire arrays.

Figure 2.3 shows schematic of the SNAP process. The AlGaAs/GaAs superlattice is created by molecular beam epitaxy (MBE) with thickness dimension control down to 10 nm, and the mold is formed by a selective etch of the AlGaAs superlattice. With an e-beam evaporator a thin chromium (Cr) layer is coated only on GaAs fingers, forming Cr nanowires whose line widths are determined by the thickness of the GaAs layers, and the separation between wires is defined by the thickness of the AlGaAs layer. Afterwards the superlattice is inverted onto an adhesive epoxy layer on silicon wafer, and the Cr wires are attached to the epoxy layer with the selectively etched away GaAs fingers. Finally an O_2 plasma RIE is used to remove the residual epoxy between Cr wires. The fabricated Cr

wires can be used as another mask to transfer the pattern into silicon substrate to form silicon nanowires.

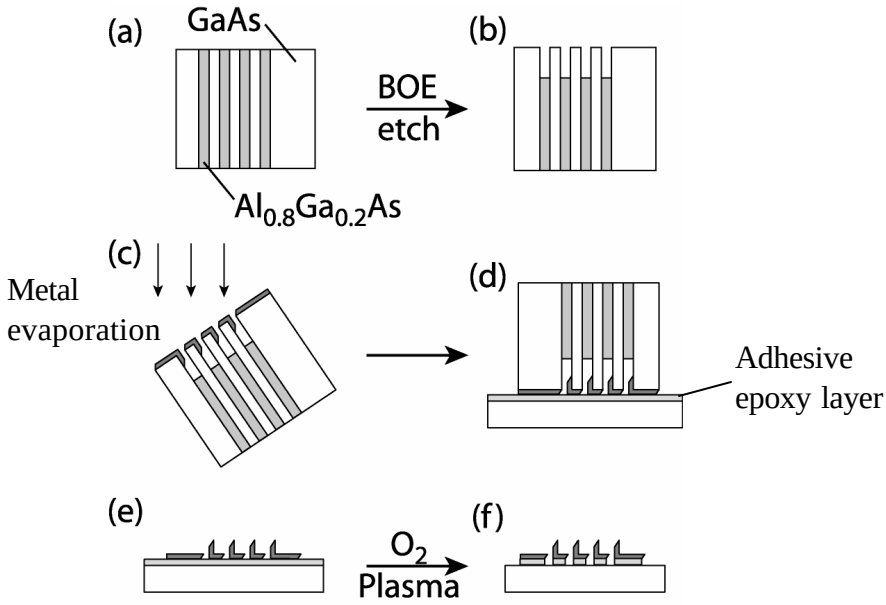


Figure 2.3 Schematic of the superlattice nanowire transfer pattern process. (a) The AlGaAs/GaAs superlattice, (b) after selective etching AlGaAs, (c) Metal deposition while superlattice tilted, (d) Invert superlattice onto adhesive epoxy layer on silicon, (e) Release of metal wires by selective etching off GaAs fingers, (f) Removal of the residual adhesive layer by RIE [27].

A similar process to fabricate some silicon nano-structures, based on the Melosh's method, was set up in our laboratory to repeat the process. A brief process flow is show in the following:

1) Cut the GaAs/AlGaAs wafer in the cleavage plane to produce 2 mm by 2 mm pieces;

2) Inspect cleaved edges of the pieces, discard those that are damaged and clean the remaining pieces with ultra-sonic cleaning. Swab the edges carefully with swabs to make sure there is no particle on the cleavage plane; (Note: The yield of this step was < 30%)

3) Dip in a diluted Buffered Oxide Etchant (BOE) (100ml BOE, 500ml H_2O) for 15 seconds to selectively etch AlGaAs. Immediately blow water off the edge; Figure 2.4 shows the scanning electron microscope (SEM) image of an example of GaAs fingers on the surface of edge after etching;

4) Evaporate a 12nm Cr layer with superlattice tilted around 45° (or other angle depending on lattice geometry). Be careful not to touch the superlattice edge.

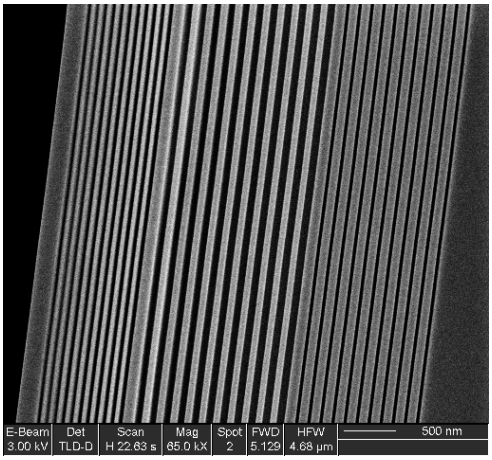


Figure 2.4 SEM image of the cross section surface of an AlGaAs/GaAs superlattice after the AlGaAs layers have been selectively etched.

5) Clean silicon substrate by Piranha solution followed by a BOE dip. Sonicate and swab substrate to remove all particulates;

6) Dispense a 15 nm adhesive epoxy film on substrate. Use epoxy bond 110, which including two parts ‘A” and ‘B. Apply 20ml tetrahydrofuran to dilute 5 drops ‘A’ and 1 drop of ‘B’ components. Filter the solution through a 0.2 micron syringe. Spin wafers to 4000 rpm at first. Drop one drop of epoxy solution onto the spinning wafer and spin for ~30 seconds. The thickness of the epoxy film formed was around 15 nm.

7) Place the epoxy film wafer onto a cold hotplate, and place the metal-coated superlattice wafer on top of the epoxy film with lattice side down. Apply pressure if desired. Turn on the hot plate to raise temperature to about 150 ºC for 30-35 minutes to cure the epoxy film. After curing, epoxy film should become an adhesive to grab the Cr wires. (Note: The yield of this step was below 50%)

8) Place the above wafers into a solution of KI(4g)/I_2(1g)/H_2O(100ml) to dissolve GaAs fingers. Typical etching time was about 12-18 hours or overnight because etchant needed to flow into the nanometric trenches to etch off the GaAs fingers. Break the superlattice free of the epoxy by pressing on the lattice side. Cr wires should be left on top of the substrate surface after removal of superlattice. (Note: The yield of this step was below 30%)

9) Using O_2 plasma, remove the residual epoxy between Cr wires.

The yield of this process (~5%) was quite low. There are two key reasons contributing to this low yield: (1) Strict requirement for cleaning. Due to the presence of micro-size particles on the side of superlattice or substrate, the contact between epoxy and Cr wires could be blocked; (2) Need a careful hand manipulation on the 2 mm by 2 mm superlattice pieces. Sometimes the sample just slipped away from a tweezer or broken due to force of grabbing, or superlattice falling down while laying on the substrate, etc. After a considerable effort, some Cr wires were finally fabricated. Figure 2.5 clearly shows the progress of our work as reflected by the SEM images of Cr nanolines as the process was improved.

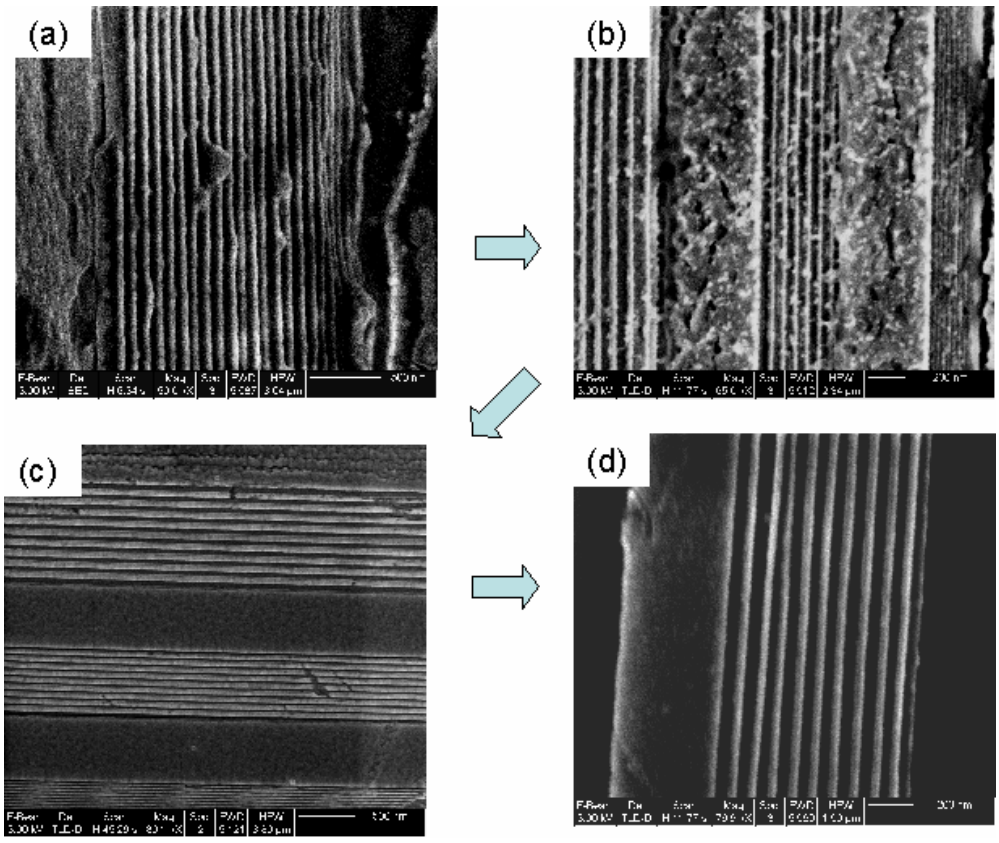


Figure 2.5 SEM images of the imprinted Cr lines as the history of process improvement. (a) The first Cr line we fabricated; (d) Cr lines after process refinement.

Besides the low yield of the samples, there was an additional issue in the subsequent RIE process. An O_2 plasma etching is needed to remove the residual epoxy between Cr wires. Because the shape of the Cr line is “L” like, it turned out that most of the time the edges of the lines collapsed during the plasma bombardment, which is shown in Figure 2.6. To address this issue, the process was modified, for example, the Cr deposition angle was changed to tailor the shape of the wire, or the RIE parameters were changed to reduce the plasma damage. After some trials the RIE results were not satisfactory. Therefore, another method was developed to directly press the superlattice

mold onto polymer film to form the polymeric nanostructure patterns. This process was similar to that of Chou *et al* developed in reference [84], which used the superlattice mold in a NIL process to pattern UV curable polymer films on a transparent substrate.

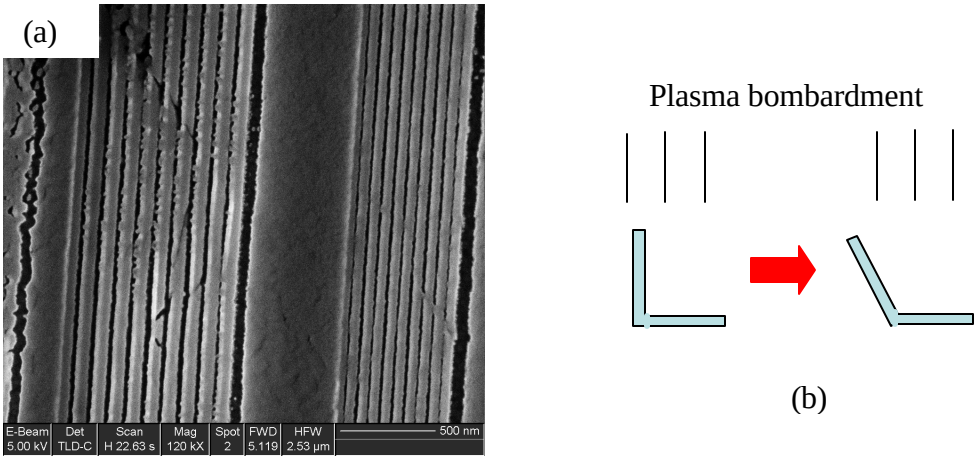


Figure 2.6 Collapse of "L" shape Cr line during plasma bombardment. (a) SEM image of Cr lines after O_2 plasma RIE etching. (b) Schematic of collapse of "L" shape lines under plasma bombardment.

B. Thermal imprinting process

In order to fabricate nanowires on silicon wafers using superlattice mold, a thermal imprint method was explored to transfer the pattern on the mold onto a polymer layer coated on a (100) silicon on insulator (SOI) wafer. The schematic of the nanoimprinting process is shown in Figure 2.7. After the BOE etching to form superlattice mold, it was treated with Hexadecanethiol or Octanethiol as a release layer to reduce the adhesion between mold and the polymer layer. A polymer layer was then spun on a silicon-on-insulator (SOI) wafer and ramped up to a set-temperature, which depended on different polymer materials. The superlattice mold was impressed into the

polymer layer and a force was applied to enhance the imprint effect. After cooling down, the mold was removed from the wafer, leading to a pattern transfer from the superlattice mold into the polymer film. Compared with the SNAP process, this method did not need a Cr coating and the subsequent GaAs etching processes, which greatly increased the process yield.

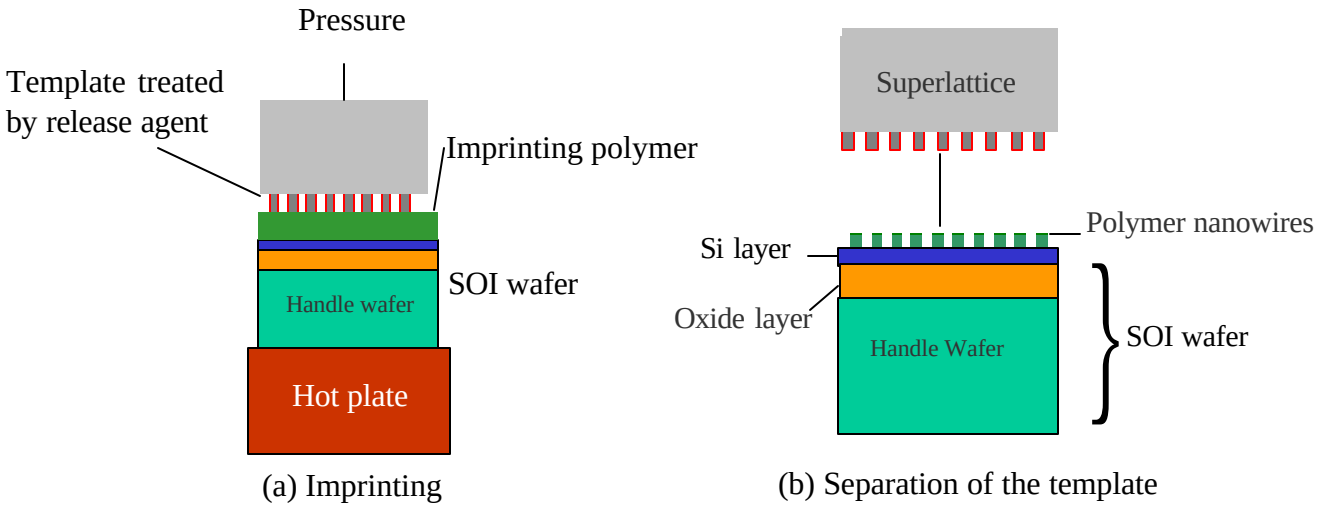


Figure 2.7 Procedure of thermal nano-imprinting process

In the process the polymer materials investigated included epoxy, Polymethylmethacrylate (PMMA), and two low-k materials such as Bisbenzocyclobutene (BCB) and Hydrogensilsesquioxane (HSQ). The investigation showed that the most efficient imprint material was HSQ due to its low viscosity and good selectivity in dry etching properties [85,86]. Epoxy and BCB were too stiff to fill in the trench of superlattice fingers even imprinted under an elevated temperature and pressure. Figure 2.8 shows SEM images of a set of BCB lines after thermal imprinting. Although the feature size could be reduced to ~10nm, the lines were very shallow, with the height only

~5 nm for the total BCB film thickness of ~60 nm. These shallow lines were not suitable for pattern transfer from polymer layer to the underlying substrate materials.

Compared with epoxy and BCB, HSQ and PMMA were much softer due to their low viscosity. Considering that PMMA is not a good mask material for pattern transfer of sub-50 nm nano-structures, HSQ was chosen for the process development. Figure 2.9 shows a cross-sectional SEM image of a set of imprinted HSQ lines. The line height was estimated to be about half the thickness of the HSQ film. The etching property of HSQ was similar to silicon oxide, which could be used as a mask material for etching small silicon structures.

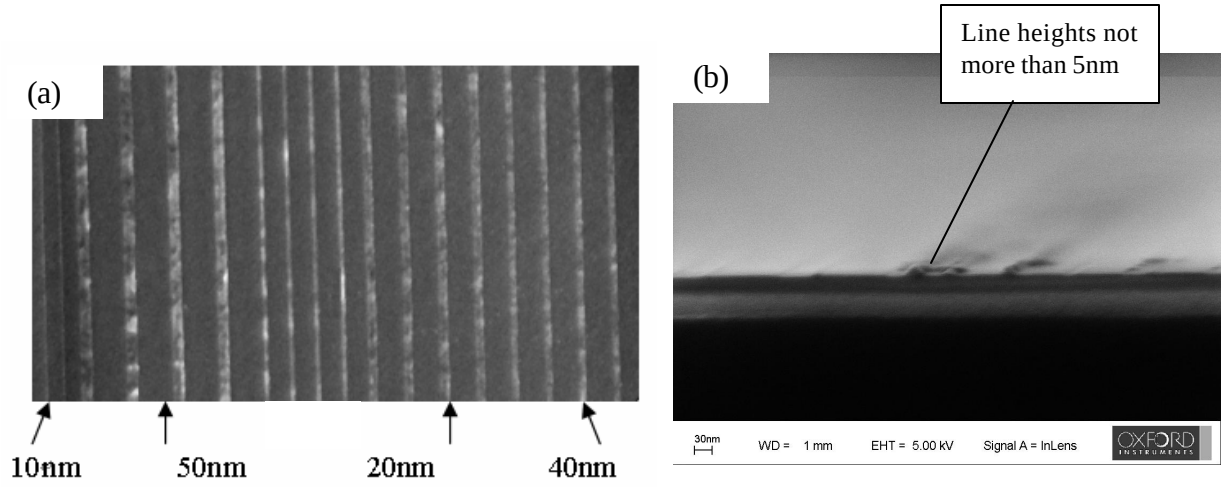


Figure 2.8 SEM images of a set of BCB lines after thermal imprinting. (a) Plan view; (b) cross-section image. The height of nanowires are very shallow.

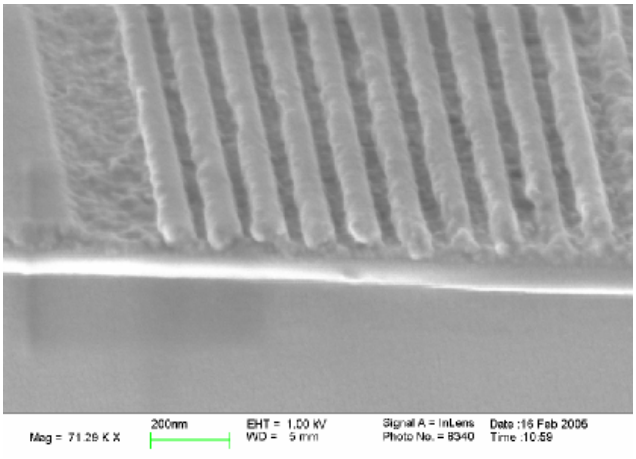


Figure 2.9 SEM image of HSQ lines after thermal imprinting. Sample was tilted 60°.

In the process, the HSQ solution was diluted by methyl isobutyl ketone (MIBK) with the ratio 1:1 to form a 40 nm HSQ film. Then the film was baked at 60°C for 5 minutes to tailor the viscosity by removing the organic solvent that was used to dilute HSQ [86]. After immersed in Octanethiol for an overnight treatment, the superlattice mold was pressed on the HSQ film for 5 minutes. In the experiment, it was found that the shape of the polymer line structures was determined by the properties of polymer and the pressure applied on the template during the imprinting. The pressure was controlled to be around 2 MPa to reduce the thickness of the polymer residual layer at the bottom of the imprinted trenches to be thinner than 15 nm. The temperature was subsequently decreased and the template was detached from the wafer, resulting in the transfer of nano-line array patterns on the polymer. Figure 2.10(a) shows SEM image of patterns imprinted on HSQ films. These lines were continuous for a length up to a few hundreds of microns. The residual polymer layer was etched by a CF_4 plasma at a pressure of 40 $x10^{-3}$ torr and RF-power of 200W until the silicon layer of the SOI wafer was exposed.

The exposed silicon layer was etched with a HBr and Cl_2 plasma down to the oxide layer using the polymer lines as a mask. Subsequently, the HSQ mask was removed in a diluted Hydrofluoric acid solution ($HF:H_2O$=1:200). Patterns with a feature size as small as 40 nm were successfully transferred to the silicon layer of SOI wafer, as shown in Figure 2.10(b).

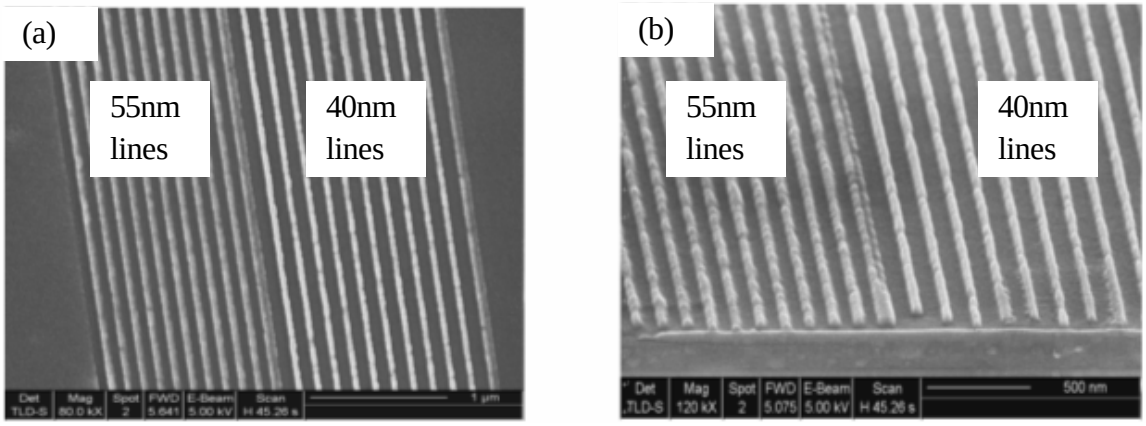


Figure 2.10 (a) SEM image of imprints on HSQ; (b) Cross-sectional SEM image of silicon nanowires after pattern transferred to device layer of SOI wafer

C. Summary of the imprinting process

In this study, the process developed by Melosh *et al* was repeated and some Cr lines were made. However, the process had a low yield and the Cr lines collapsed under plasma bombardment. Therefore, a thermal imprinting process using superlattice mold was developed, which enabled us to fabricate HSQ and silicon nanowires with feature size down to 40nm. There were three key points regarding this set of experiments:

1) The process explored used superlattice mold, which featured translating thin film growth thickness control into 2D planar wire arrays. On one hand, the method provided an effective way to form imprinting mold with feature size down to 10nm, but on the

other hand, it could not be used to form patterns other than line structures. The process lacked flexibility for test structure formation;

2) In the imprinting experiment, it was found that the shape of the polymer line or pattern thickness contrast was strongly influenced by the properties of polymer, *i.e.* viscosity or adhesion between polymer and GaAs fingers. For example, based on the Young Equation, if the interface free energy of polymer-GaAs fingers is too high compared with surface free energy of polymer or GaAs, the polymer may not be able to fill in the trenches between the GaAs fingers, which results in narrow imprints. If the interface free energy is too low, the adhesion is so good that it is difficult to neatly detach the mold from polymer. There should be a trade-off for the surface energy control. In order to form smoother and better defined wires than those shown in Figure 2.6(a), it was necessary to fine tune material properties to achieve a better control on the imprint process;

3) In the experiments, it was also found that the imprinting processes required a rigorous tuning of experimental parameters in process control. Figure 2.11 shows three typical pattern defects in the NIL process [87]. It is indicated that the imprinted patterns are directly related to geometry of mold patterns, applied force and resist properties. In practice, it was occasionally observed that the imprint at the edge area was deeper than that in the central area, which is just due to the defect mechanism in Figure 2.11(c). For a good control of imprinting process, it was necessary to fine tune the experiment parameters, such as material properties, mold pattern design and applied force on mold, etc, especially in the process to obtain nano-structures. It was also noted that for S-FIL

process, these effects were not obvious due to a liquid form of resist was used in the imprinting process.

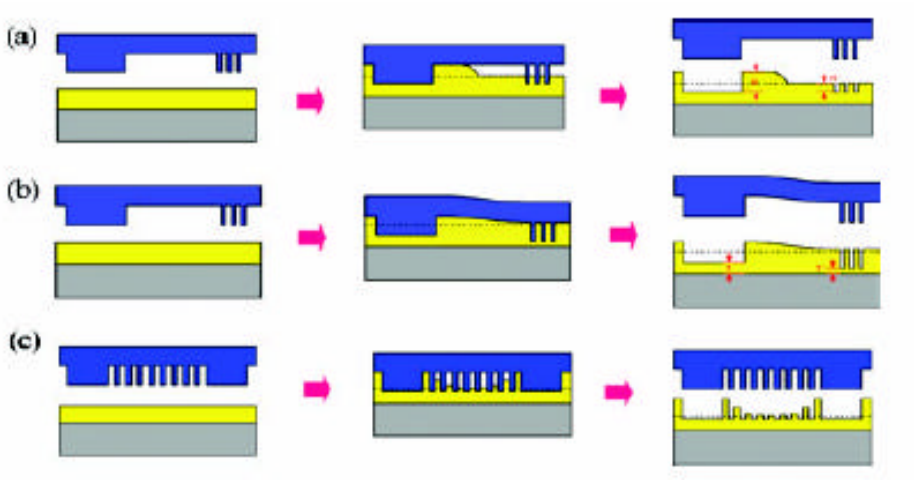


Figure 2.11 Schematic of pattern defects in NIL. (a) Inhomogeneity in imprints due to resist build-up around large feature sizes; (b) Mold bending under a large pressure, resulting in non-uniform residual thickness; (c) Incomplete pattern replication due to central area of mold not being completely filled in [87].

Besides NIL process, e-beam lithography technique was also explored as another method to obtain nano-structures. The results are shown in the following section.

2.1.2 E-beam lithography (EBL)

Electron beam lithography (EBL) is widely used to form ultra small patterns, for example, silicon-Germanium quantum dots [88], silicon pillars [26], sub-100 nm copper interconnects [89], etc. Due to the small wavelength of e-beam, the primary advantage of EBL is to overcome the diffraction limit of light and make features in the nanometric regime. In the EBL process, e-beam resists are the recording and transfer media of the designed nano-structures. The resist is spun on a substrate to form a coating layer, which

is then baked to remove the residual solvent. The resist layer is then subjected to electron irradiation, which modifies the microstructure of the resist, leaving it either more soluble (positive tone) or less soluble (negative tone) in developer. After developing, the pattern is transferred to the substrate by a selective etching process (RIE or wet etching).

In this part, we first discuss specimen layer stacks for fabrication of nano-structures, including a discussion on resist layer thickness and the use of chromium layer as conductive layer. Then some details in the EBL tests performed in the lab are investigated, including dose level test, proximity effect and stitching errors. Finally, a summary and a brief comparison between EBL and the thermal imprinting process will be presented.

A. Layer stacks in EBL

There are two issues to which attention needs to be paid in the production of high resolution patterns. The first issue is the control of resist thickness. It is known that a thinner resist layer is desired to obtain ultra small nano-structures. For example, in reference [90] Word *et al* successfully fabricated grating structures with a pitch as narrow as 27 nm on HSQ resist layer with only 30 nm thickness. However, a thicker resist layer is required to transfer the resist pattern into the substrate by selective etching process. Therefore there is a trade-off of the resist thickness between the requirement of resolution and the capability of pattern transfer. In our experiment a ~130 nm thick resist layer was used to fabricate sub-50 nm features. Another issue is the exposure of resist on insulating substrates. Substrate charging may cause pattern distortion when patterning resist layer

directly on insulators or even on semiconductors. A simple solution for exposure at higher energies (>10 kV) is to evaporate a thin metal layer on top of the substrate, to distribute electron charge during e-beam exposure [91]. A ~15 nm thick Cr layer was employed as a conductive layer in the EBL process. Figure 2.12 shows a typical layer stacks on top of silicon substrate, where SiO_2 layer serves as a buffer layer between Cr layer and substrate to prevent the formation of Cr silicide.

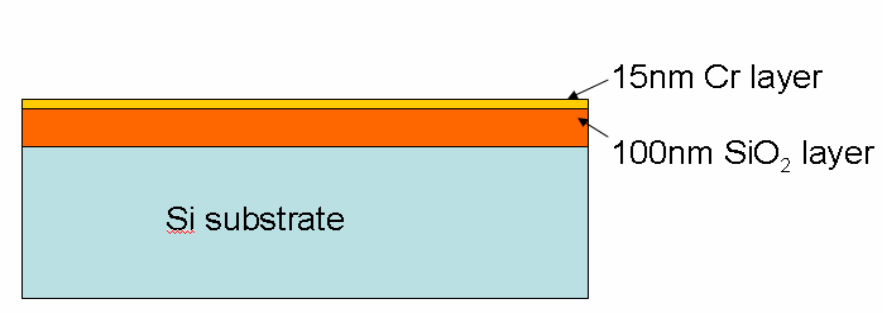


Figure 2.12 Schematic of layer stacks on silicon substrate

The EBL experiments were conducted with a JEOL JBX6000 e-beam writer at the UT Microelectronic Research Center. The system is capable of patterning small areas on 4" substrates, and a 6" diameter area on an 8" substrate. A positive tone e-beam resist ZEP-520a, which consisted of a copolymer of chloromethacrylate and methylstyrene, was used to record the designed patterns. In a typical EBL tests, Zep-520a was first diluted by a solvent ZEP-A with the ratio 1:1, and the solution was spun on the wafer at 3500 rpm for 120 seconds to obtain a ~130 nm thick resist layer. After baking at 180°C for 2 minutes to remove the solvent, the resist layer was subjected to an exposure of electron beams with 50keV energy per electron under a specific dose. After immersion in a

developer ZED-N50 for 90 seconds and a subsequent rinse by Isopropyl Alcohol (IPA), the designed pattern appeared in the resist layer.

B. Dose level test

For an e-beam writer it is very important to perform a dose level test to determine the optimum dose to apply, because feature dimension is directly related to e-beam exposure dose and the instrument condition may vary after a period of time. The dose for a good pattern transfer may be somewhat constant; however, the exposure process may affect the actual dose received. For example, the dose may be different when there is a conductive layer underlying the resist layer to distribute electron charges. The dose will also vary with resist thickness. Typically under the same condition, a lower dose is required to expose a thinner resist layer. The standard dose for undiluted Zep-520a resist is 180 $\mu C/cm^2$ and 0.12 nC/cm. In the EBL process the real exposure dose is set to add or subtract an additional percentage based on this standard dose. For example, a -60% dose means the real dose is (1+(-0.6))*standard dose. In the dose design, we use the additional percentage of standard dose, for example, -60%, as an indicator representing the exposure dose level. A typical dose test design includes a series of patterns with various feature sizes, which are subjected to e-beam exposure under a set of different doses. Figure 2.13 shows a set of SEM images of resist lines that underwent e-beam exposure with different doses. When the dose level was low, which is shown in Figure 2.13(a) with a -70% dose, under-exposure occurred on the fine line patterns because the dose was not enough to expose the whole resist layer between lines. As dose increased to -60%, too much dose

might effectively reduce the feature dimensions, resulting in an over-exposure as shown in Figure 2.13 (b). Thus according to this test, dose around -65% may be a suitable level for the formation of a sub-50nm resist pattern, which is shown in Figure 2.13 (c).

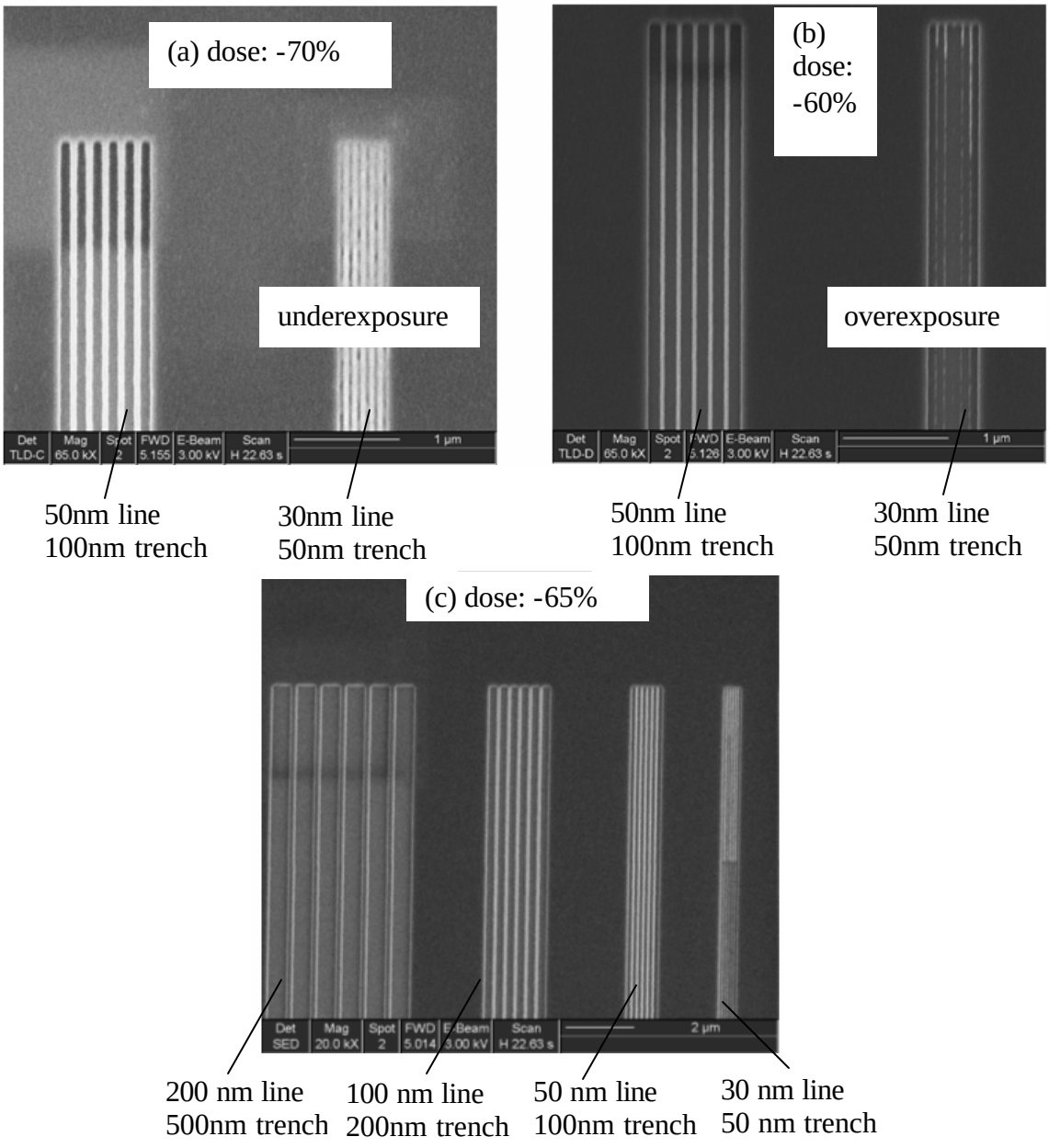


Figure 2.13 SEM images of resist patterns after a dosage test. (a) dose: -70%; (b) dose: -60%; (c) dose: -65%. The dimensions below the images are the designed values, which may not be the real dimensions due to different dose levels.

Figure 2.14 shows the results of the measured line width vs. dose level for a set of designed line patterns. It is clearly indicated the obtained linewidth decreased as the dose level increased. It is also noted that compared with the large feature size, the linewidths of narrow lines such as 50 nm lines, was influenced more strongly by overdose level, indicating a necessity to precisely control dose in the fabrication of ultra-fine structures.

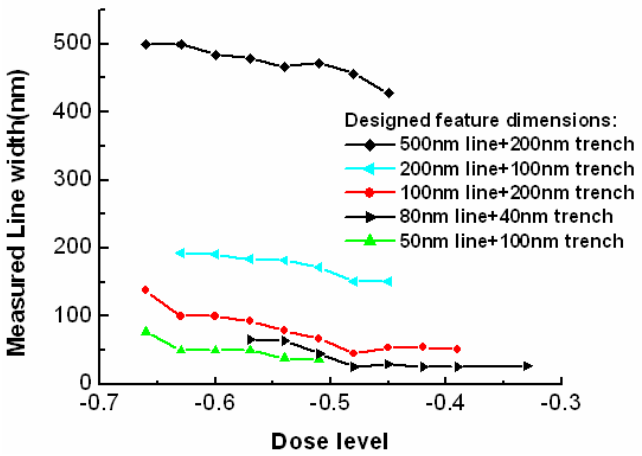


Figure 2.14 Measured line width (by SEM) vs. dose level for a set of designed patterns. It is shown that as dose level increased, feature dimension decreased due to overexposure.

In some cases over-exposure might be an effective method to obtain features that is smaller than the designed dimensions, which is shown in Figure 2.14 for 50 nm lines and 100 nm lines. However, a large overdose may introduce severe side effects in EBL, including proximity effect and stitching errors [92,93], which will be discussed briefly in the following.

C. Proximity effect and Stitching errors

In EBL, the resolution may be limited by scattering of electrons in resist and substrate. These electron scattering effects, often referred to as the proximity effect [92],

affect exposure of outer areas surrounding the area of incident beam. Typical electron beam lithography tools use electron beams with 10-100 KeV energy per electron. In the exposure, the electrons can easily penetrate the resist layer and reach the substrate and experience multiple scattering events, which may result in significant variation of the pattern written from the intended size. For periodic nano-structures filled in a large area, the dose level of the central area is different from that of the corner or side area due to the proximity effect, which may leads to non-uniformity of feature size in the exposed area. For example, Figure 2.15 shows a SEM image of a nano-grating structure with linewidth around 50 nm. The feature size of pattern central area is smaller than that of side area due to the proximity effect, resulting in a contrast difference in SEM imaging.

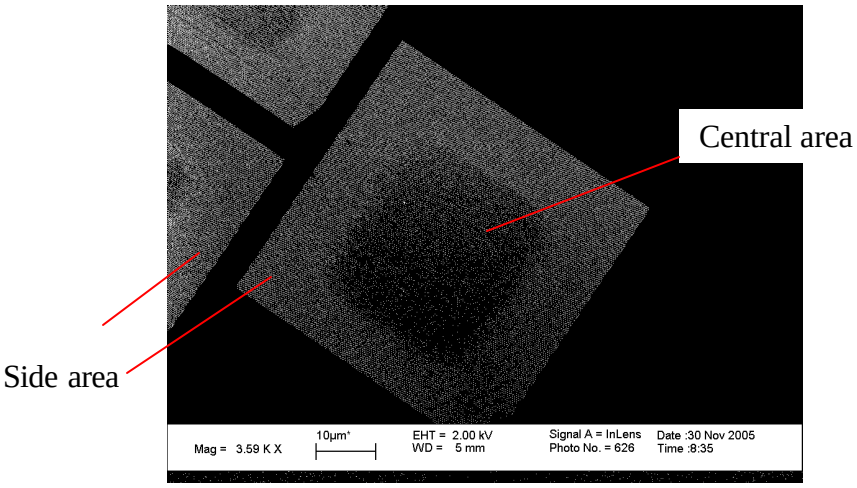


Figure 2.15 SEM image of a nano-grating structure with grating around 50nm. The feature size of pattern central area is smaller than that of side area due to the influence of proximity effect, resulting in a contrast difference in SEM imaging.

In order to reduce the proximity effect, it is better to use a low dose in the writing so that the electron scattering is reduced. Meanwhile, a modification of designed pattern can also mitigate the influence of proximity effect. For example, in the formation of a

grating structure, the feature size of the central area is deliberately designed to be somewhat larger than that of side area. The magnitude is dependent on the severity of proximity effect which is determined from trial and error.

In EBL systems, all the large-area patterns are formed by stitching together a mosaic of small fields or stripes [93]. Interfield stitching errors, the unintended discontinuities which occur at the boundaries between adjacent fields due to overdose at interfield area, are one of major contributors to pattern errors in EBL. Figure 2.16 shows a typical SEM image of nano-structure influenced by stitching errors. At the boundary of two fields the 40 nm lines are discontinuous due to overdose at the interfield area. In our experiments, because the field size was 80μm by 80 μm, the written patterns are deliberately designed to be within each field to overcome this problem. And generally it is suggested that a lower dose in the writing would be better for reducing the influence of stitching errors.

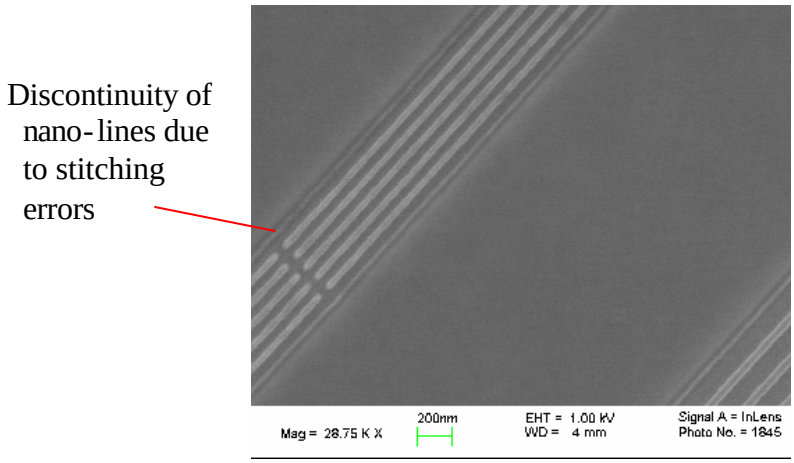


Figure 2.16 SEM image of a set of 40nm nano-lines. Discontinuity occurred at the interfiled area due to stitching errors.

Therefore, in the EBL experiments we first performed dose test, then used SEM to investigate written patterns to examine the exposure effect. The dose level was normally determined to be just slightly higher than the right dose, ensuring the full exposure of resist layer but without significant proximity effects and stitching errors. Then we modified the designed pattern to tailor the feature size accordingly, and conducted EBL tests again. After some trial and error runs, the patterns and the dose conditions were determined, which enabled satisfactory patterns to be obtained with yield close to 100%. Figure 2.17 shows two cross-sectional SEM images of two sets of nano-lines after patterns transferred to silicon substrate. It is shown that patterns with feature sizes of 50 nm and 100 nm were successfully transferred to the silicon substrate. Compared with nano-lines fabricated with thermal imprinting process in Figure 2.10, these nano-lines with EBL processes had comparable feature sizes but the yield was much higher.

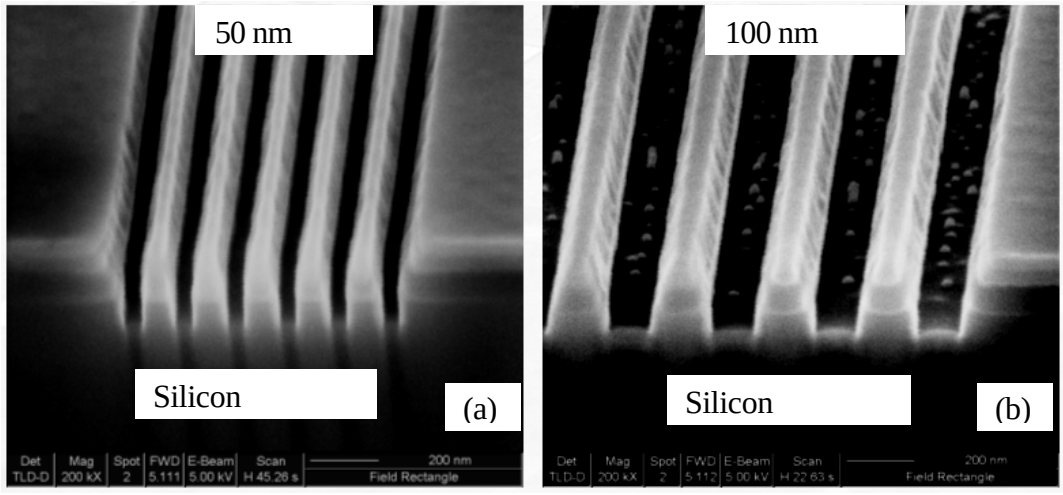


Figure 2.17 Cross-sectional SEM image of two sets of nano-lines after pattern transferred to silicon substrate. (a) 50 nm lines; (b) 100 nm lines

D. Summary

With the EBL technique, after performing dose level tests, silicon nano-structures with feature size around 50 nm were successfully obtained. There were three main advantages of electron beam direct-write technique: (a) Flexibility towards design change and no need of a mask, which enable us not only to form nano-structures, but also fabricate the corresponding test structures; (b) The resolution was good in forming nano-structures with feature size smaller than 50 nm, and the ZEP resist had the required selectivity in the pattern transfer; (c) Once the patterns and dose conditions were properly-defined, the yield of the process was close to 100%. One of the major drawbacks of EBL is the inherent low throughput due to the serial exposure in the process. For example, an exposure of a 1 mm by 1 mm square may take 5 hours of tool time, depending on the dose level and the gun current. Thus, in the industry, electron beam lithography is used mainly to generate exposure masks to complement conventional photolithography or nano-imprinting lithography. In this study, because only a low volume production of the test structures were needed, EBL instead of thermal imprinting was our preference to fabricate nano-structures, mainly due to its high resolution, high yield and high flexibility of design change.

2.2 Pattern Transfer Techniques

In order to form silicon-based nano-structures, patterns in the resist layer need to be transferred directly into the substrate or into a thin film, which may in turn be used as a mask for subsequent etches. The objective of pattern transfer is to selectively remove material using patterned resist as a masking template. For a successful pattern transfer, there must be sufficient selectivity (etch-rate ratio) between the material being etched and the masking material. Typical pattern transfer techniques for silicon nano-structure formation include dry etching [29, 80], lift-off [88] and anisotropic wet methods [31,33]. Table 2.1 shows some wet and dry etchants of mask materials for silicon pattern formation [80].

Pattern transfer is of critical importance in achieving the desired quality of the silicon nano-structures. In the following, first we explored the dry etching processes in MRC, which are normally used to form silicon nano-structures. Afterwards we performed a brief investigation of the use of the lift-off process for pattern transfer. It is followed by an introduction to a fabrication process combining AWE and optical lithography. The latter process was developed in NIST to form CD reference materials [31]. In the summary, it is shown that among the three techniques, the quality of the fabricated silicon structures with AWE process was the best, as evidenced by the form of the cross-sectional profile. With these results, it is proposed to develop a process to combine AWE and EBL to not only form high quality silicon nano-structures, but also further reduce feature size to sub-45 nm dimensions.

Table 2.1 Wet and dry etchants of some mask materials for silicon pattern formation [80]

	Wet Etchants (Aqueous Solutions)	*Etch Rate (nm/min)*	*Dry Etching Gases (Plasma or Vapor Phase)*	*Etch Rate (nm/min)*
Thermal silicon dioxide	HF	2,300	CHF_3+ O_2	50–150
	5 NH_4F:1 HF (buffered HF)	100	CHF_3+ CF_4 + He	250–600
			HF vapor (no plasma)	66
LPCVD silicon nitride	Hot H_3PO_4	5	SF_6	150–250
			CHF_3 + CF_4 + He	200–600
Aluminum	Warm H_3PO_4:HNO_3: CH_3COOH	530	Cl_2 + $SiCl_4$	100–150
	HF	4	Cl_2+ BCl_3 +$CHCl_3$	200–600
Gold	KI:I_2	660		
Titanium	HF:H_2O_2	110–880	SF_6	100–150
Tungsten	Warm H_2O_2	150	SF_6	300–400
	$K_3Fe(CN)_6$:KOH: KH_2PO_4	34		
Chromium	$Ce(NH_4)_2(NO_3)_6$: CH_3COOH	93	Cl_2	5
Photoresist	Hot H_2SO_4:H_2O_2	>100,000	O_2	350
	CH_3COOH_3 (acetone)	>100,000		

(*After:* [3, 4].)

2.2.1 Dry etching process—Reactive ion etching (RIE)

Reactive ion etching (RIE), which is widely used in semiconductor industry and scientific study to form small structures, consists of bombarding the material to be etched with chemically reactive ions. In a RIE chamber, chemical ions are generated using plasma discharge to break reaction gas molecules, and then react at the surface of material being etched to form volatile products, which are evacuated from chamber by a pumping system. Typical reaction gases include oxygen, fluorine-based gases such as CF_4 or CHF_3, chlorine and bromine based gases such as Cl_2 or HBr. For example, in MRC O_2 is normally used for etching or ashing polymeric residues, CF_4+O_2 based plasma are often used to etch oxide, nitride, W or Ti, Cl_2+O_2 gas mixture are used to etch Cr, and

$HBr+Cl_2$ plasma is normally used to selectively etch silicon. In the following section, a dry etching process was developed to form silicon nano-structures.

In plasma etching techniques, etching rate and selectivity are two important controlling parameters. Selectivity is the ratio of etching rates between two different materials in the same plasma. In RIE of silicon nano-structures, in MRC an $HBr+Cl_2$ plasma is normally used to selectively etch into silicon substrate. Instead of using resist as a mask, Cr or SiO_2 are the two most common mask materials used in the Si RIE process due to their good selectivity in silicon etching. Since a Cr layer is favored for usein the EBL process as a conductive layer for charge control, the resist patterns formed by EBL process need to be first transferred into Cr layer. After some trial and error runs, the optimized recipe for Cr etching was developed, using Cl_2+O_2 plasma with the flow rate of Cl_2 and O_2 to be 9.7 standard cubic centimeters per minute (sccm) and 2.25 sccm, respectively. The chamber pressure was 80 mTorr and the radio frequency (RF) power for plasma generation is 75W. Under this condition the etching rate of Cr was about 15nm/minute. The selectivity of Cr to Zep resist was about 1:3.3, indicating at least 50 nm resist layer was required for the pattern transfer. Normally to ensure a full breakthrough of Cr layer and for a good Cr sidewall profile after etching, a 100% overetch is needed in the plasma selective etching [91]. Therefore the minimum Zep resist layer thickness was ~100nm. In the current process, usually a ~130 nm thick resist layer was employed to ensure that the pattern was reliably transferred from resist into Cr masks.

After Cr etching, normally a CHF_3+O_2 plasma was used to etch through the underlying oxide layer, which served as a buffer layer to prevent the formation of chromium silicide. Then there are two possible methods to transfer pattern into the silicon substrate, depending on whether Cr or SiO_2 was used as the hard mask material in the RIE process. One was to use patterned Cr as a mask for opening the oxide thus permitting it to be used for pattern transfer to the silicon substrate. After the silicon substrate etch, the chrome and oxide layers are then removed with a Cr etchant and Buffered Oxide Etch (BOE), respectively. Another method was etching the Cr only, then transferring the pattern to the oxide, removing residual chrome, and finally using the oxide as the mask for pattern transfer into silicon. Both of the methods could be used to fabricate silicon nano-structures, but the sidewall profiles after etching were quite different, which was attributed to different anisotropy in RIE process with different masks.

Anisotropy in RIE refers to preferential erosion in a direction normal to the surface of a wafer. When Cr is used as a mask, it serves as a hard mask in the silicon RIE process because Cr does not react with HBr+Cl_2 plasma to form volatile products and would not be removed by ions except that caused by physical bombardment. For SiO_2, the selectivity of Si to Oxide in the etching condition is close to 20:1, indicating the oxide layer to be still a soft mask. Figure 2.18 and Figure 2.19 show the SEM images of a set of silicon lines obtained by HBr+Cl_2 plasma etching using oxide and Cr as masks, respectively. The silicon lines are ~60 nm wide and ~250-300 nm high. Compared with the trapezoidal cross-sections in Figure 2.18, the cross-sectional profile in Figure 2.19 is more close to a rectangular shape, indicating a better anisotropy etch control when using

Cr as a hard mask. It is also noted that in both etching processes, the sidewalls of silicon lines were not smooth and possessed some wave-like traces, showing the occurrence of plasma damage during dry etching processes.

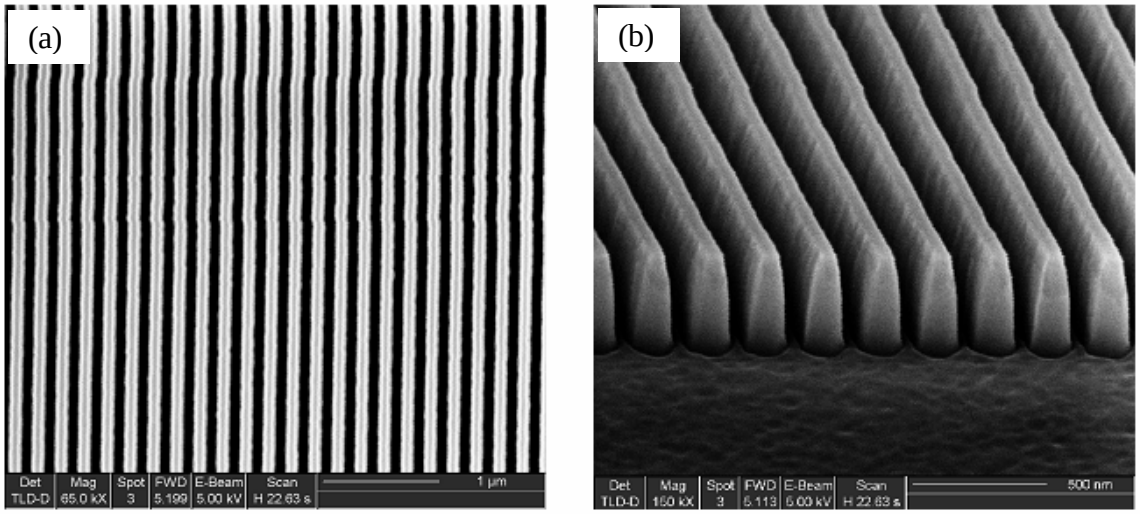


Figure 2.18 SEM images of a set of Si lines fabricated by HBr+Cl_2 RIE using silicon oxide as mask. Line width is ~60 nm. (a) Plan view image; (b) Cross-sectional image with sample tilted 60°. Lines are trapezoidal shape after RIE etching.

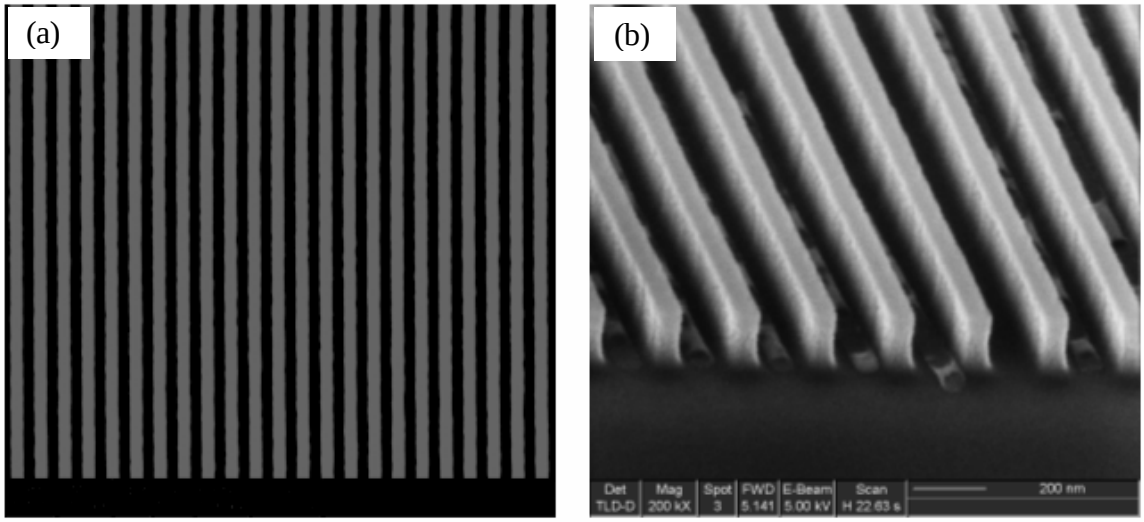


Figure 2.19 SEM images of a set of Si lines fabricated by HBr+Cl_2 RIE using Cr as mask. Line width is ~60 nm. (a) Plan view image; (b) Cross-sectional image with sample tilted 60°. Lines are rectangular shape after RIE etching.

Similarly, fluorine-based gases such as CF_4 and CHF_3 could not etch Cr since the chromium fluoride products are solids at room temperature. Chrome can be also used as a mask material for selectively dry etching silicon oxide or nitride. Due to its more suitable etching behavior, Cr is widely used as a mask for pattern transfer in the fabrication processes. From Figure 2.17 to Figure 2.19, it is shown that silicon nanolines could be successfully fabricated with feature size ~ 60 nm and aspect ratio ~ 4 by RIE process.

2.2.2 Lift-off process

Lift-off process is a method for patterning films that are deposited, typically used for transfer of the resist pattern to a corresponding metal pattern [26, 94]. Instead of etching, in the lift-off process a metal such as Au or Cr is first evaporated onto the resist pattern, covering both the resist area and the area in which the resist has been removed. Then a specific solvent such as acetone or resist stripper is used to undercut and wash away the resist as well as the metal film on top of the resist, resulting in the formation of a metal pattern left on the area where the film was deposited directly on the substrate. It is noted that the formed metal pattern is reverse to the resist pattern.

In the experiments, after EBL a 15 nm Cr was coated on top of the Zep resist pattern by e-beam evaporation. In the actual lift-off process, a solution made of deionized water (DI): Ammonium hydroxide (NH_4OH) : Hydrogen peroxide (H_2O_2) =5:1:1 was applied to remove the resist and take away the Cr film above it. Figure 2.20 shows a set of 50 nm Cr lines fabricated by lift-off process, and the corresponding silicon lines after selectively dry etching using these Cr lines as masks. It is found in Figure 2.20(a) that

some Cr residue still left after the lift-off process, indicating that more process control is needed to obtain a cleaner lift-off.

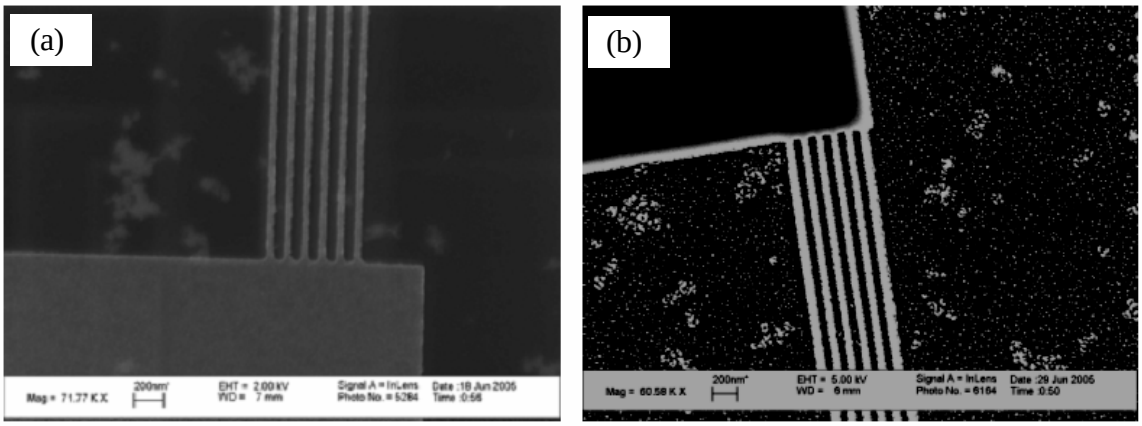


Figure 2.20 Plan view SEM images of Cr lines and Si lines fabricated by lift-off process Line width is ~50 nm. (a) Cr lines, some Cr residue still left after lift-off; (b) Silicon lines fabricated by $HBr+Cl_2$ RIE using Cr lines as masks.

2.2.3 Anisotropic wet etching process

Another pattern transfer technique is to use the lattice-plane anisotropic wet etching properties of some silicon etchants. Silicon etching solutions such as tetra-methyl-ammonium hydroxide (TMAH) or KOH remove silicon from the {111} lattice planes at a rate much slower than they etch other planes, thus allowing the {111} planes of the silicon to behave as lateral etch stops. Based on this phenomenon, silicon anisotropic wet etching has been widely used to fabricate high-aspect-ratio nanostructures with smooth and flat sidewalls [31,32,95,96]. Furthermore, under the situation of using (110) silicon substrate, in the special case when features of a test structure are lithographically aligned with <112> directions in the (110) silicon wafer surface, under optimum conditions, they are replicated with vertical and nearly atomically flat sidewalls

by (111) lattice-plane selective-etching. Figure 2.21 shows a SEM plan view image and a cross-sectional low resolution transmission electron microscope (LRTEM) image of silicon nano-lines, which were fabricated at NIST by i-line lithography of the wavelength of 365 nm and anisotropic wet etching (AWE) process [95]. It is shown that the silicon nano-lines were straight and have vertical and almost flat sidewalls. Compared with Si lines obtained by dry etching in Figure 2.19, these lines had a much better quality.

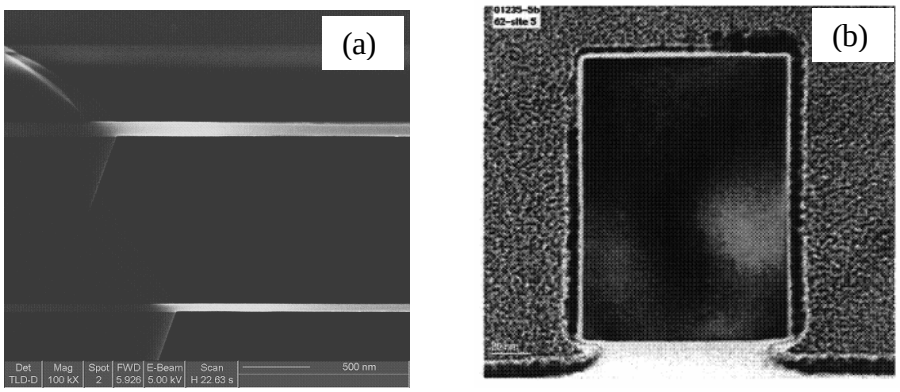


Figure 2.21 (a) SEM images of Si nanolines in device layer of (110) SOI wafer fabricated by AWE. (b) HRTEM cross-sectional image of a silicon line [95]. Lines are straight having vertical and smooth side walls.

2.2.4 Summary

For fabrication of silicon nano-structures, the resist pattern as defined by EBL needs to be transferred to the silicon substrate. A chromium layer was used as a conductive layer in EBL as well as a mask layer in the following selective RIE process. Two processes including RIE and lift-off were explored for the Cr pattern formation from the Zep resist pattern. $HBr+Cl_2$ plasma etching was successfully used to selectively etch silicon to obtain silicon nano-structures with feature size around 50nm. Then a process developed by NIST was introduced, which combined optical lithography with AWE, to

obtain silicon CD reference materials. Compared with the structures fabricated by RIE process, the silicon lines by AWE process were straight and had well defined line profile with vertical and flat sidewalls. In the following section, a process to combine AWE and EBL is described which is used to form both high quality silicon nano-structures and further reduce feature size to the sub-45 nm region.

2.3 Combination of EBL and AWE

The general process sequence for the fabrication of silicon nano-structures is shown in Figure 2.22. The process began with a 15 nm chromium coating by an e-beam evaporator on (110) silicon wafers already having an oxide layer deposited on their upper surfaces by low pressure chemical vapor deposition (LPCVD). The 15 nm chromium layer was used as a conductive layer for charging control during the EBL process as well as a hard mask for patterning the oxide layer by a RIE process. The oxide layer in turn served as a mask in TMAH etching for pattern transfer to silicon. After chromium evaporation, a positive-tone resist was spun on the wafer to a nominal thickness of 130 nm. The resist was imaged on an electron-beam exposure system operating at 50 kV. In the exposure, for a rough alignment at first, the horizontal features in Figure 2.22 were aligned with the cleavage edge of the (110) wafer, which is close to the <112> crystalline orientation. Pattern transfer from the resist to the chromium lines was performed by a Cl_2 and O_2 plasma at a pressure of 80 x 10^{-3} Pa and an RF-power of 75 W for 2 min. The exposed oxide layer was etched in a CHF_3 and O_2 plasma down to the (110) silicon surface using the chromium lines as the etching mask. Subsequently, the residual resist

was removed in a Piranha solution, and TMAH heated to 80°C was used to etch silicon along (111) planes. Finally, the chromium and oxide layers were removed by Transene Chromium Etching Solution 1020 and buffered oxide-etching solution, respectively.

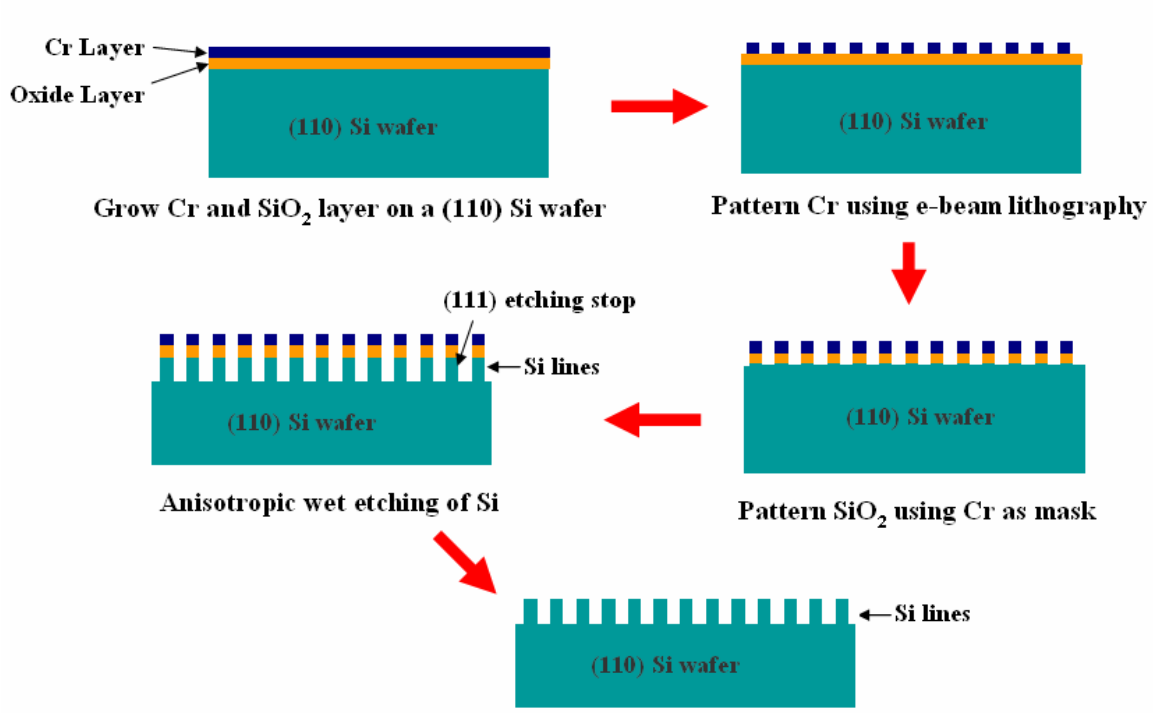


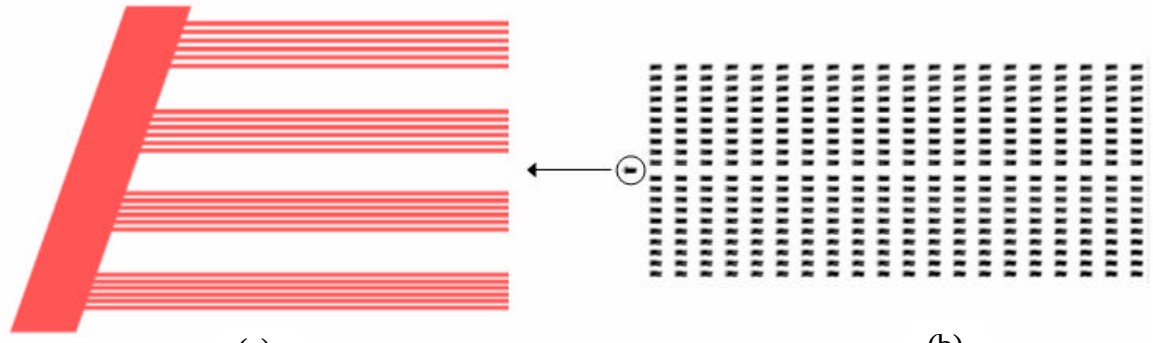
Figure 2.22 Process sequence for fabrication of silicon nanolines by EBL and AWE.

In this process, the challenge of using TMAH for AWE was the requirement for precise orientation alignment at the nano-metric scale, which required the feature edges to be aligned with the <112> crystalline direction on (110) silicon wafer. This enables the formation of vertical and smooth sidewalls after a (111) lattice-plane selective-etching. The following part focuses on how to deal with orientation alignment to obtain features with tens of nanometers by the AWE process.

2.3.1 Orientation alignment

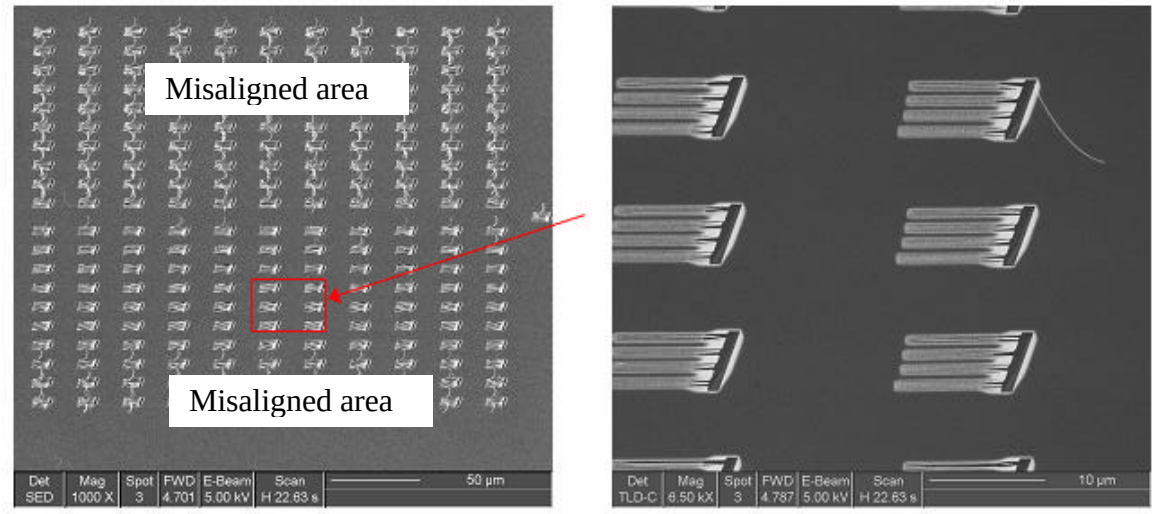
Orientation alignment is of critical importance to the fabrication of silicon nanostructures using AWE technique, particularly for long and narrow silicon nanolines [32]. As a rough alignment, feature edges were first aligned to the cleavage edges of (110) silicon wafer, which was nearly along [112] orientation. This alignment was not precise enough to form good quality silicon nanolines, especially for the process aimed at the level of tens of nanometer. For fine alignment, a test structure was designed to identify the effect of proper orientation alignment and misalignment, which is shown in Figure 2.23. The test structure here was a pattern array repeating the same pattern but with different directions. Figure 2.23(a) shows the unit pattern, including four sets of nanolines with a step of linewidth of 10 nm. In this pattern the dark areas corresponded to those that were exposed to the electron-beam and then removed by the developer. The white areas were those where silicon remained after lattice-plane selective etching. A trench was located at one end of the lines, to facilitate the cross-sectional SEM imaging after AWE. In Figure 2.23(b) the same unit pattern was repeated 20×20+1 times with different directions. For example, assume that the direction of the pattern that is circled is 0°. In this array the directional difference of each pattern from its horizontal adjacent neighbor is 0.01°, and the directional difference of the pattern from its vertical neighbor is 0.2°. The direction range of the array is from -2° to 2° with a 0.01° step. The idea of this test structure design was that the nanolines with the best quality, having the most smooth sidewalls and widest linewidths, can be obtained with one of the patterns that had the proper orientation alignment.

Figure 2.24 shows two SEM images of silicon nanolines with Cr mask still on top after the AWE process. In Figure 2.24(a) it is noted that in the misaligned area, some of Cr lines peeled off due to the undercut of silicon in AWE. It is shown that only with proper alignment the Cr lines could remain on surface, which is shown in Figure 2.24(b). From the observation of the etching effect on test structures by SEM imaging, the direction with proper orientation alignment could be determined. Figure 2.25 shows a set of silicon lines fabricated after removal of Cr and Oxide masks. They show that feature size as narrow as approximately 40 nm were successfully patterned in the silicon substrate. The features were straight and well defined with vertical and flat sidewalls. The heights of these silicon lines were above 520 nm indicating the formation of features with aspect ratios of more than 13:1. The quality of the line profile could also be used to judge the quality of orientation alignment.



(a) (b)

Figure 2.23 The orientation test structure that was designed to investigate the effect or orientation alignment. The dark areas correspond to those of the positive resist that are exposed to the electron-beam and are then removed by the developer. The white areas are those where silicon remains after AWE. (a) The unit pattern. The pattern includes four set of nanoline structures with a step of linewidth of 10nm. A trench pattern was specifically put at one end of the lines, to facilitate the cross-sectional SEM imaging after AWE; (b) Pattern array for observing the effect of alignment. Each pattern in the array has different direction, and the step of direction is 0.01°.



(a) (b)

Figure 2.24 SEM images of silicon nanolines with Cr on top surface after AWE. (a) Overview of the test structures after AWE. In the misaligned area, some of Cr lines peeled off due to the undercut etching of silicon in AWE. It is indicated that only with proper alignment that Cr lines could remain on surface, which is shown in (b).

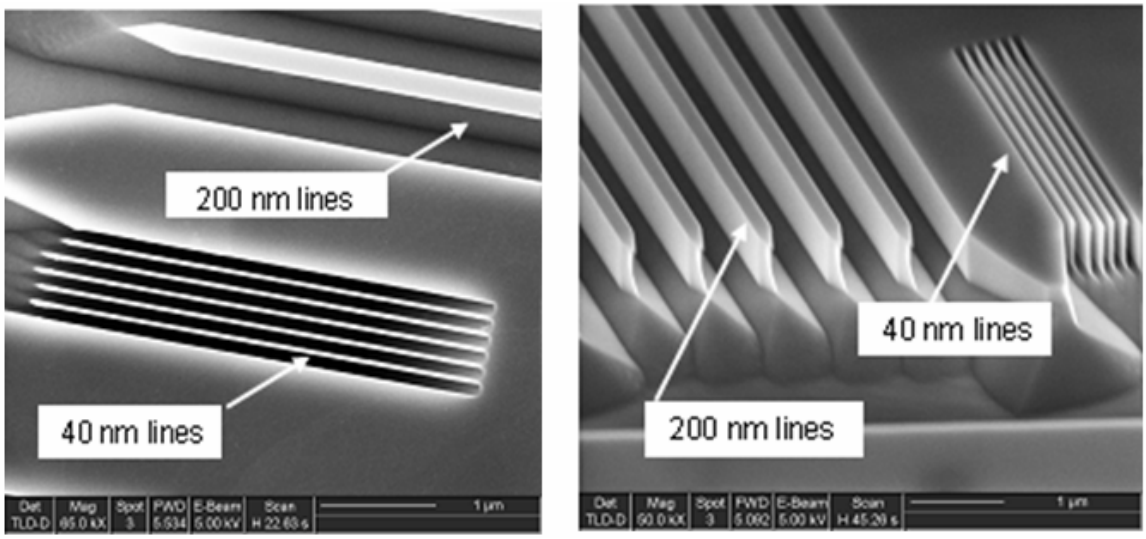


Figure 2.25 SEM image of Si nanolines fabricated by EBL+AWE. (a) Plan view image; (b) Cross-sectional image.

For silicon nanostructures fabricated by AWE, under an orientation misalignment condition, wet etching occurred along different {111} crystalline planes, which could result in two effects on the silicon nanolines obtained. One is multi-step formation in the line direction on the sidewalls. This effect may influence uniformity of nanolines. Another effect is that the feature size comes out smaller than designed, in which the difference is dependent on the degree of the misalignment. Figure 2.26 shows two SEM images with improper orientation alignment during AWE. In Figure 2.26(a), linewidth was only ~ 50nm instead of 90nm of the designed value. As the degree of misalignment increased, the lines finally collapsed as shown in Figure 2.27(b), with multi-steps appeared along the length direction on the sidewalls. This led to a roughing of sidewalls.

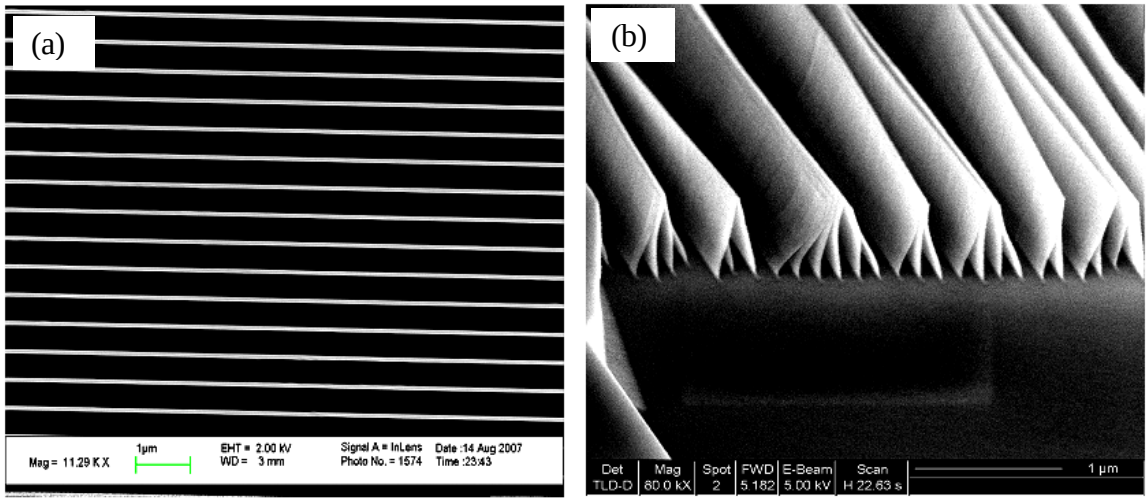


Figure 2.26 SEM images of two sets of Si lines fabricated by EBL+AWE with improper orientation alignment. (a) Plan view SEM image of one set of Si lines with misaligned angle around 0.5°. Linewidth is around 50 nm. (b) Cross-section image of another set of Si lines with misaligned angle around 1°. Steps appeared on the sidewalls. Moreover, in (b) nanolines collapse due to a larger misalignment.

Figure 2.27 shows a plot of linewidth vs. misaligned angle for a set of nanolines after AWE process, indicating that mis-alignment etching reduced the feature size of the fabricated nano-structures. It is shown that linewidth reduced as misaligned angle increased. Meanwhile, it was noted that as misaligned angle was smaller than a specific angle, ~ 0.4° in this case, the change of linewidth is only around 16%, from 90 nm to 75 nm in this test. As the misaligned angle increased to beyond 0.4°, the rate of change increased, leading to a ~ 40% decrease of feature size with another 0.2° misalignment. As the misaligned angle increased to 0.7°, nanolines finally broke at the center after etching.

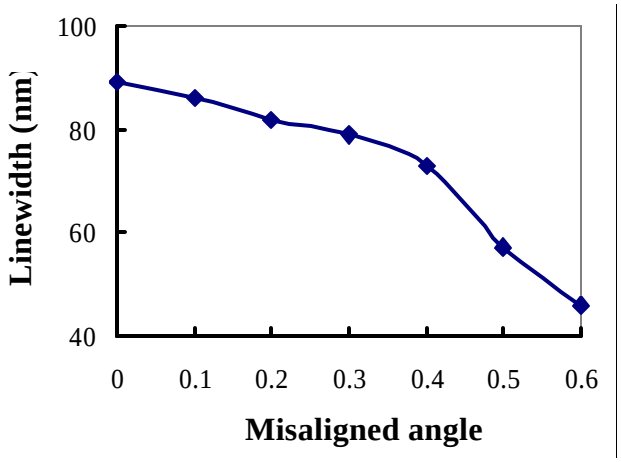


Figure 2.27 Plot of linewidth vs. misaligned angle for a set of SiNLs after AWE process.

In summary, from this set of experiments it is shown that misorientation alignment results in multi-step formation at sidewalls, non-uniformity of nanolines and loss of feature size after wet etching. This influence is more serious for narrower nanolines, and if the roughness introduced by multi-steps at the sidewalls was comparable to the linewidth, nanolines could collapse or break due to the large misalignment. A proper alignment includes two steps: the first is a rough alignment of feature edge along with the cleavage plane of silicon wafer, which is close to [112] crystalline direction, and the second step is a fine alignment by observing the etching effect on the orientation test structures with SEM imaging, including the peeling off of Cr mask lines, breakage of narrow silicon lines, etc, to find the best quality silicon nanolines with the smoothest line edges and the fattest linewidth. The developed process was able to fabricate silicon nano-structures with feature size as small as 40nm and aspect ratio above 12, which is shown in Figure 2.25. In the application of the AWE processes, an orientation test structures similar to Figure 2.23 was always included to determine the proper direction for orientation alignment.

2.3.2 Fabrication of Silicon Nanolines on (110) Si wafer

The mechanical properties of silicon nano-structures play an important role in controlling the functionality and reliability of the nano-scale devices, since silicon-based nanostructures are essential building blocks for nanoelectronic devices and NEMS. In order to perform mechanical tests at nano-metric scale, some silicon nanoline arrays have to be fabricated in order to investigate its mechanical response under an applied load.

A typical structure design for the fabrication of nanoline arrays is shown in Figure 2.28. In this test, we simplified the fabrication process by including in the design a 10 by 8 structure arrays with the direction change from -0.4 to 0.4 degree with a step of 0.01°. The length of nanolines was from 30μm to 60μm, depending on the requirement of experimental tests. To mitigate the proximity effect in EBL, the linewidth of the central areas of each unit pattern was deliberately designed to be slightly larger than that of side areas. The distance between each unit pattern was set to be 160 μm, which was twice the field size of 80 μm. This made the e-beam writing of each unit pattern being inside one single field in order to avoid the stitching errors. After the EBL and AWE process, the proper direction with the best orientation alignment was determined by observing the etching effect of the orientation test structure. Then in the nanoline pattern arrays the corresponding structure with the proper direction was found, which represented the structure with the best orientation alignment and had the best quality of nanolines. This pattern array also enabled the investigation of the effect of mis-orientation angle on the nanoline geometry after the AWE process.

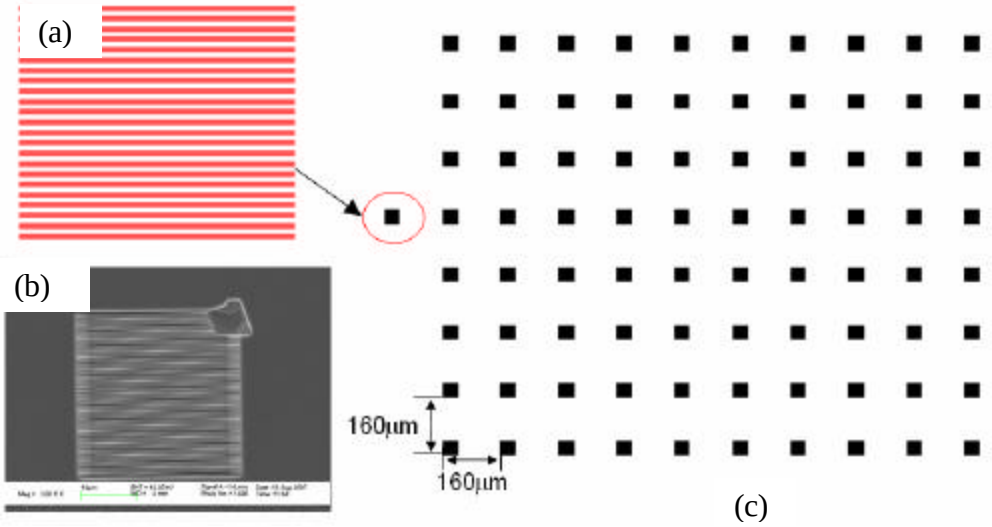


Figure 2.28 The silicon nanoline arrays fabricated by EBL and AWE. The dark areas correspond to those of the positive resist that are exposed to the electron-beam and are then removed by the developer. The white areas are those where silicon remains after AWE. (a) The unit grating pattern; (b) SEM image of the unit silicon grating structures after AWE. A trench pattern is specially designed at one corner of the line to facilitate the cross-sectional SEM imaging. (c) Pattern array for orientation alignment. Only the best aligned structure has the best quality of silicon nanolines.

Figure 2.28(b) shows a plan-view SEM image of a unit silicon nanoline array after AWE. A trench pattern was specially designed at one corner of the line to facilitate the cross-sectional SEM imaging. Figure 2.29 shows SEM cross-sectional images of three sets of silicon nanolines fabricated by EBL+AWE. The linewidth of nanolines varied from 30 nm to 1500 nm, and the height of the lines ranged from 360-1000 nm, which was controlled by TMAH etching time and etching temperature. The good crystal quality and well-defined geometry, along with the smooth sidewalls and the highly uniform line width, made these silicon nanolines well suited for accurate mechanical measurements as well as numerical modeling.

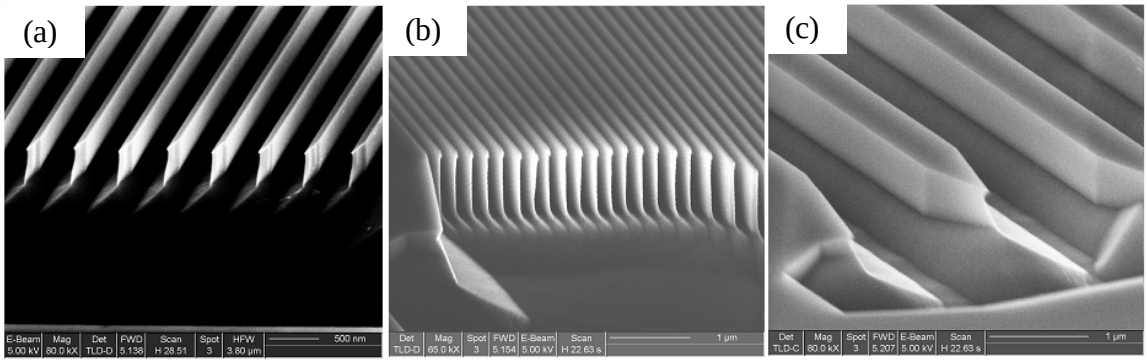


Figure 2.29 Cross-sectional SEM images of some Si nanoline arrays fabricated by EBL+AWE. (a) 30 nm wide lines with height of ~ 350 nm; (b) 65nm wide lines with height of ~ 1 µm. (c) 1500 nm wide lines with height of ~ 560 nm. A trench pattern as shown in Figure 2.28(b) is specially designed at one corner of the nanoline to facilitate the cross-sectional SEM imaging, showing the sharp edges due to the anisotropic etching.

2.3.3 Fabrication of Silicon nanolines on (110) SOI wafer

The developed process can also be applied to fabricate silicon nano-structures on (110) SOI wafers, where the buried oxide layer serves as an etching stop layer in the formation of some electrical test structures. In the following section, some process modifications will be described for the fabrication of silicon nanoline structures on SOI wafer, which could be used for electrical transport study of NiSi nanolines by reacting a nickel layer that was deposited onto the silicon nano-lines. Generally, the fabrication process flow was similar to that on (110) silicon wafer, but more careful and precise control was required due to the structure difference between the (110) SOI wafer and the bulk silicon wafer.

The (110) SOI wafer was purchased from SOITEC, having a ~70 nm thick silicon (110) device layer and ~150 nm buried oxide layer on a (100) handle wafer. Figure 2.30

shows a cross-sectional TEM images of the layer stacks of the (110) SOI wafer, indicating a 67 nm silicon layer on top of 149 nm buried oxide layer.

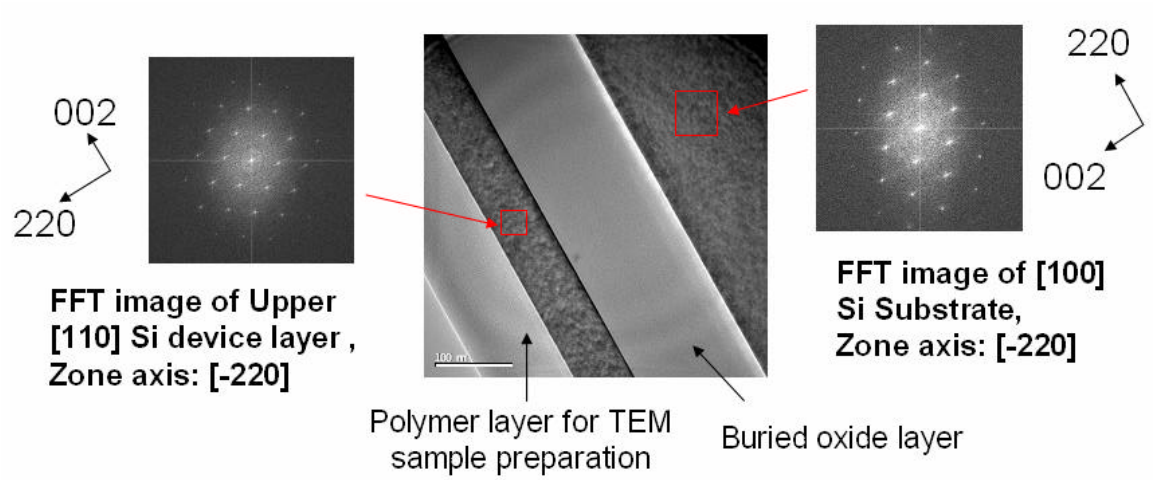


Figure 2.30 A cross-sectional TEM image of the layer stacks of the (110) SOI wafer, the Fast Fourier transform (FFT) image of the (110) device layer and the FFT image of the (100) silicon substrate. The left-bottom part is the top surface of SOI wafer. It is shown that the [220] orientation of (100) substrate, which defines one of the cleavage edges of the SOI wafer, is parallel to [002] orientation of (110) device layer. Meanwhile, the zone axis of the (100) substrate, which determines another cleavage edge of the SOI wafer, is [2-20] and is parallel to [2-20] zone axis of the (110) device layer.

From the two Fast Fourier transform (FFT) images of the (110) device layer and the (100) silicon substrate, it is clearly shown that the [220] orientation of the (100) substrate, which defines one of the cleavage edges of the SOI wafer, is parallel to [002] orientation of (110) device layer. Meanwhile, the zone axis of the (100) substrate, which determines another cleavage edge of the SOI wafer, is [2-20] and is parallel to [-220] zone axis of the (110) silicon device layer. Therefore, compared with (110) silicon wafers, the cleavage edges of this set of SOI wafers are nearly along [002] or [-220] orientation in (110) silicon device layer, instead of along [112] orientation in (110) silicon wafers.

This difference requires a modification on the orientation alignment in the fabrication process.

For this purpose, the pattern is needed to rotate to some specific angles, which are the direction difference between <112> crystalline direction and the cleavage edges of SOI wafer. Figure 2.31 shows the layout of orientation alignment in the fabrication of silicon nanolines on SOI wafer. Since the cleavage edges were determined to be either [002] or [-220] orientation of the device layer, the rotation angles should be the angle difference between them and [112]. Figure 2.31 (a) shows a schematic of orientation relationship in a (110) silicon crystalline plane, suggesting two possible rotation angles of either 35.3° or 54.7°. Accordingly the design of the orientation test pattern was modified, and the SEM image is shown in Figure 2.31 (b). This pattern included four similar sub-patterns for orientation test, which are rotated by either ±35.3° or ±54.7°. Each of the sub-patterns was similar to the design as shown in Figure 2.23 that are used for orientation alignment of (110) bare silicon wafers. The idea of this design was that even if the exact orientation along the cleavage edge was not known, two of the four sub-patterns would meet the orientation requirement and generate good quality nanolines after wet etching. Figure 2.31 (c) and (d) shows two SEM images including a misaligned structure after AWE, showing Cr lines peeled off due to undercut in wet etching, and a set of nanolines with proper alignment. In this specific case the rotation angle is 35.3°, indicating the cleavage edge is aligned with [002] orientation of the (110) silicon device layer.

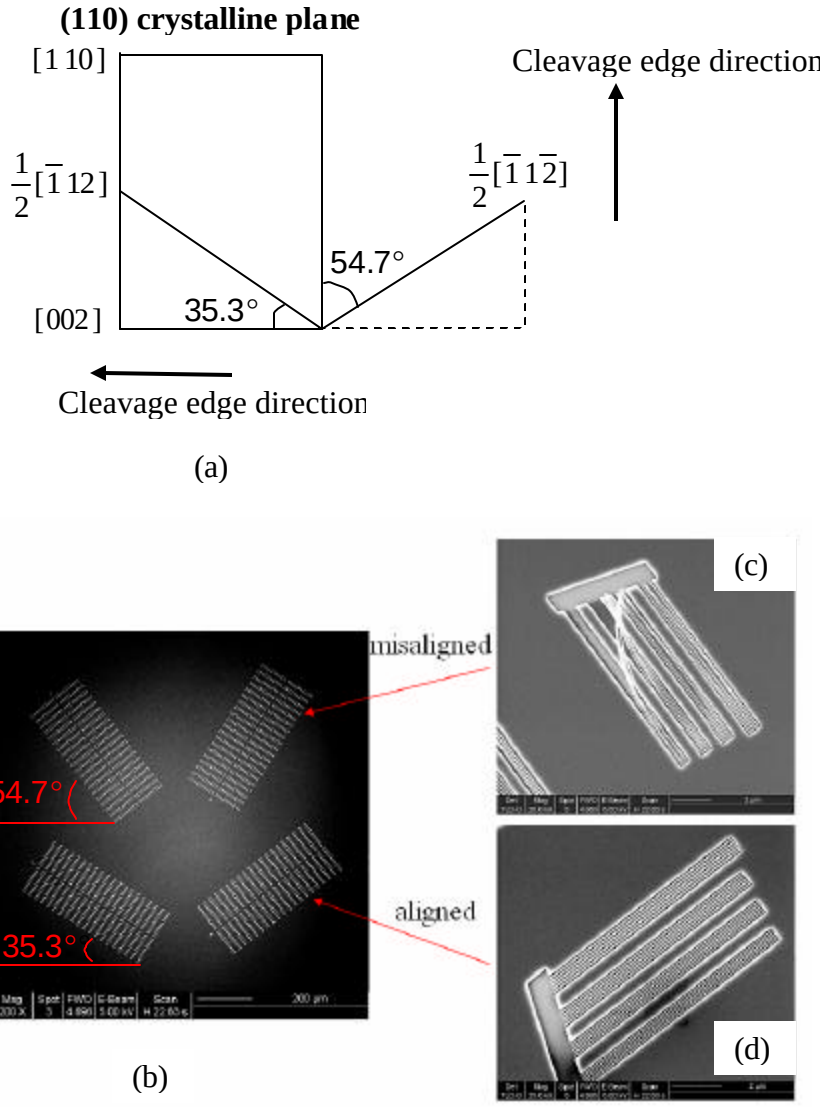
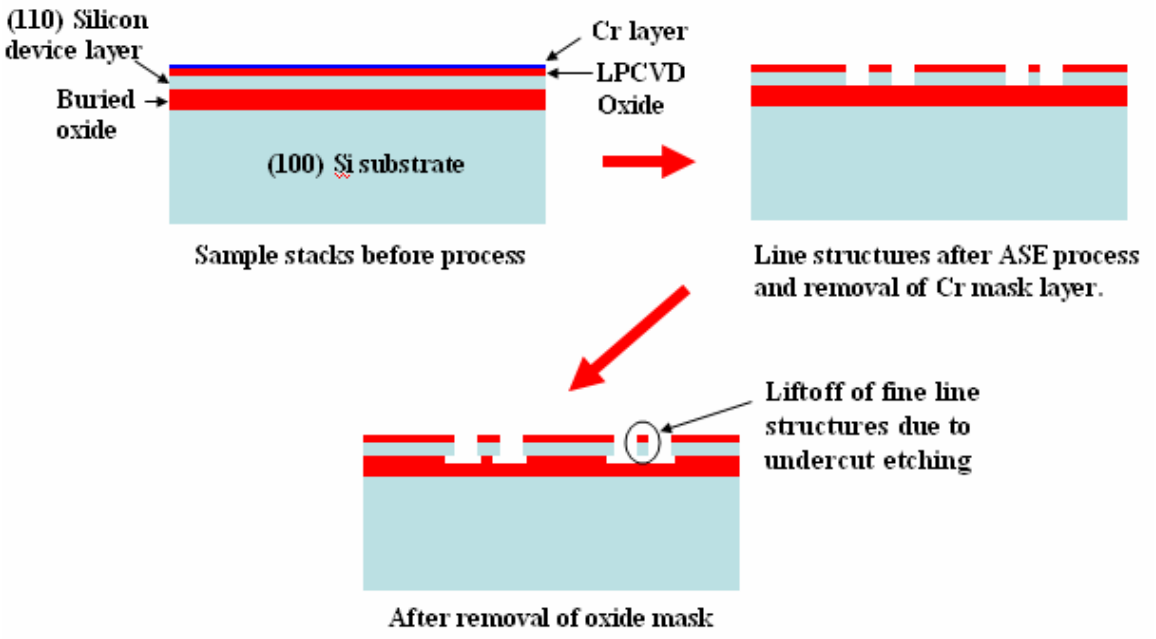


Figure 2.31 Orientation alignment in the fabrication of silicon nano-structures on SOI wafer. (a) Schematic of orientation relationship in a (110) silicon crystalline plane; (b) SEM image of the orientation test pattern on SOI wafer, including four same test patterns that are rotated by either ±35.3° or ±54.7°, respectively. (c) SEM image of a misaligned structure after AWE. Cr lines peeled off due to undercut in wet etching. (d) SEM image of a set of nanolines with proper alignment.

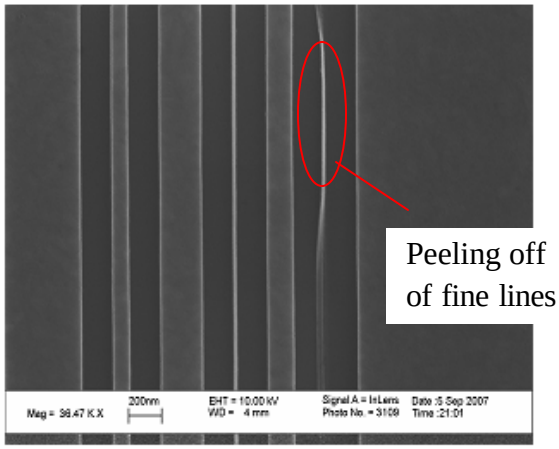
Besides the orientation alignment, another concern in the formation of silicon nanolines on SOI wafer was the "lift-off" of fine lines after the removal of oxide masks by BOE etching. As shown in the diagrams in Figure 2.32(a), after AWE, Cr etchant and BOE were needed to remove Cr and Oxide masks. During the BOE wet etching, the etchant would remove both the oxide mask on top of silicon nano-lines, and the buried oxide beneath the nanolines. This can lead to "lift-off" of fine lines due to an undercut etching of buried oxide, which is shown in the SEM image of Figure 2.32(b). In order to address this issue, a precise control of the thickness of the oxide layer between the Cr layer and the (110) silicon device layer was needed, which was not necessary for the previous fabrication process on (110) silicon wafer. Typically a 9 nm oxide layer was grown between Cr layer and silicon device layer, to avoid the reaction between Cr and silicon. After the AWE process and removal of Cr mask by Cr etchant, a $CHF_3 + O_2$ plasma etching was used to thin down the thickness of the oxide layer to ~ 3 nm, which was then removed by a very short dip in diluted BOE. The effect of the BOE dip was to both fully remove the residual oxide layer and to clean the surface of silicon after the plasma etching.

After the improvement of the fabrication process, silicon nanolines were successfully fabricated on (110) SOI wafer by wet etching. Figure 2.33(a) shows a SEM image of a set of silicon nanolines formed in the silicon device layer. The linewidths of these lines ranged from ~ 20 nm to ~ 100 nm. The line height was determined to be ~ 67 nm by atomic force microscope (AFM) imaging as shown in (b) and (c). Here the buried oxide layer served as an etching stop layer during the AWE process. The nanolines were

straight and uniform, with feature size down to ~20 nm, which were well suited to electrical or thermal transport study in tens of nano-metric scale.



(a)



(b)

Figure 2.32 (a) Diagram of "lift-off" of fine line structures due to undercut wet etching after removal of Oxide mask. (b) SEM image of a set of silicon nanolines fabricated on SOI wafer. Fine line with linewidth around 20 nm peeled off due to undercut etching.

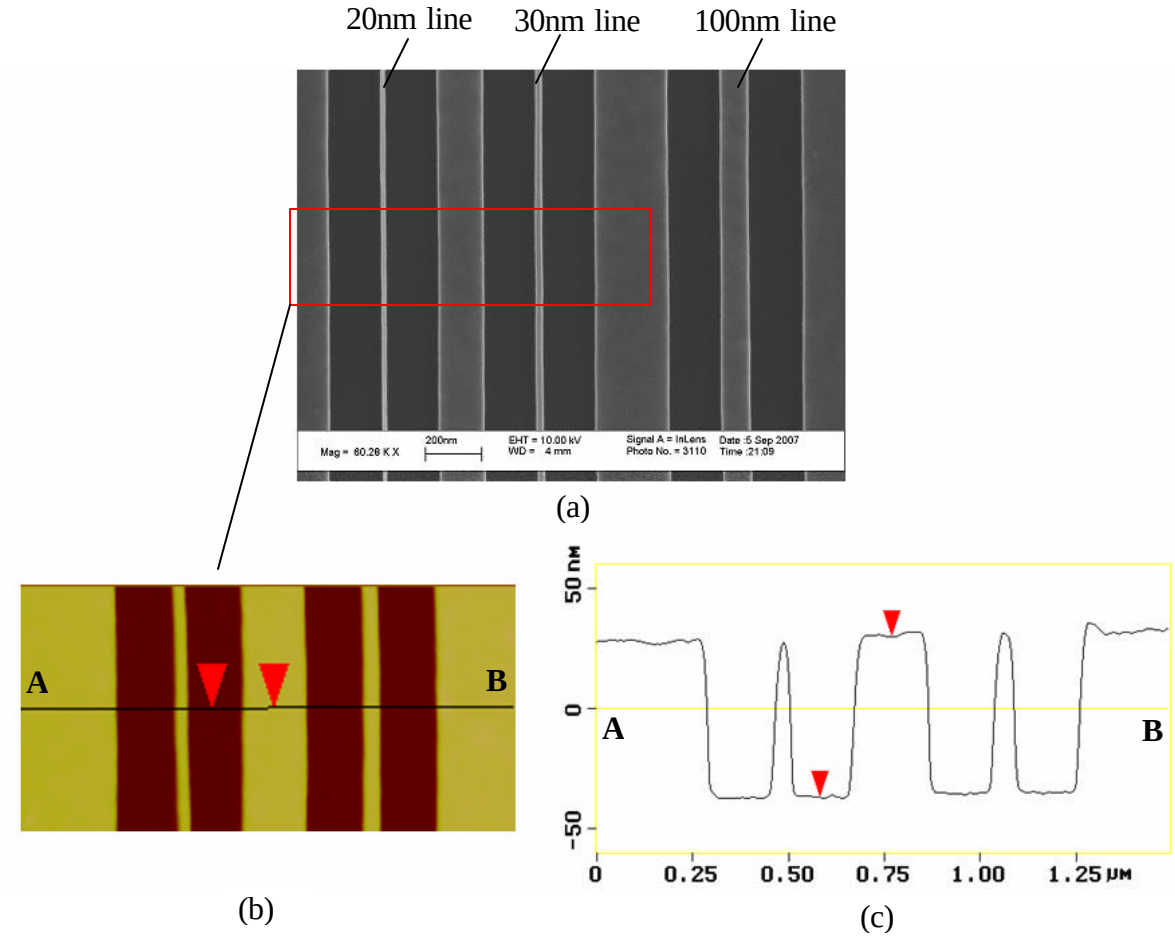


Figure 2.33 (a) plan view SEM image of a set of silicon nanolines fabricated on (110) SOI wafer. Linewidths were around 20 nm, 30 nm and 100 nm, respectively. Lines were straight and uniform after wet etching. (b) AFM image of the selected area showed the height of lines are ~ 67 nm, according to the line profile from A to B in (c).

2.4 Summary

This study demonstrates for the first time the feasibility to fabricate single-crystal Si nanolines by combining electron-beam lithography with an anisotropic wet etching process. With this process, it was possible to fabricate silicon nanoline arrays on (110) wafer with feature size down to 30 nm. The height of lines varied from ~300 nm to ~1500 nm, depending on the TMAH etching time and temperature. These silicon

nanolines could be used for mechanical study in a nanometric scale, which will be discussed in Chapter 3 and Chapter 4. The fabrication process could also be used to form silicon nano-structures on (110) SOI wafers, where the buried oxide layer served as an etching stop layer. Silicon nanolines with feature size down to ~20 nm was successfully fabricated in the device layer of SOI wafer, with line height was determined by the thickness of the silicon device layer (~ 67 nm in Figure 2.33) . This set of silicon lines could be used to form electrical test structures for electron transport study of nickel silicide in nanometric scales, which will be discussed in Chapter 5. The fabricated single crystalline silicon nano-lines were straight and have well-defined dimensions, having nearly atomically flat sidewalls with almost perfectly rectangular cross sections and highly uniform linewidth. The good quality of these nanolines makes them well suited for accurate experimental measurements at tens of nanometer scales.

There were still remaining concerns in this fabrication process. The first concern was about the control of line height, which was dependent on the TMAH etching time and temperature. Compared with a normal dry etching process, the wet etching was relatively fierce, typically at a rate of around 1.2 μm per each minute at 90°C. Sometimes a shallow etching was needed to control the height of nanolines to be around ~100 nm, for example, etching at a low temperature or in a short time. One problem is that during the AWE with a mild etching, some hillocks might appear on the surface of nanolines. Figure 2.34 shows a SEM image of a set of silicon nanolines about 40 nm wide and 150 nm height, which underwent only ~15 seconds of TMAH etching. It is noted that there are some hillocks existed on the lines, possibly due to an insufficient wet etching. A

better way for height control was using (110) SOI wafer, where the height of nanolines was controlled by the thickness of the device layer. The inconvenience was that (110) SOI wafer was much expensive than (110) silicon wafer, plus it was not easy to find the right SOI wafers since the source of these wafers was limited.

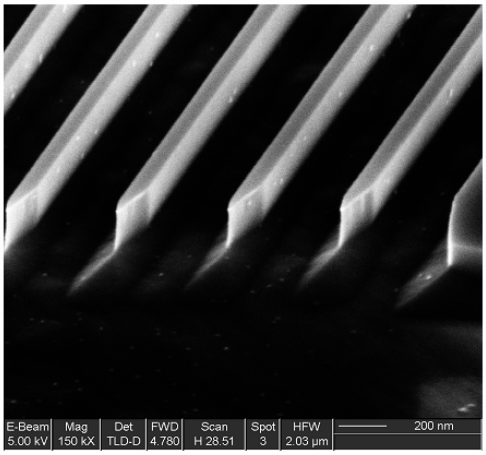


Figure 2.34 Cross-sectional SEM image of a set of Si nanoline arrays fabricated by EBL+AWE. Linewidth is ~40 nm and line height is ~150 nm. Hillocks appeared on the surface of lines, possibly due to an insufficient strong etching.

Another concern was about the orientation alignment for narrow silicon nanolines, for example, nanolines with feature size below 20 nm. A simple estimation of the requirement of orientation alignment for nano-metric scale silicon lines is the following: assume that the length of silicon lines is L nm, and misaligned angle is θ. In a perfect orientation alignment the misaligned distance through the whole line length direction should be smaller than the crystalline plane distance of [112], which is 2.22 **?**. Thus we have

$$L\sin\theta \cong L\theta \leq 2.22\text{?} \qquad \textbf{(2.1)}$$

When silicon lines was 5 μm long, θ should be less than 0.0025° and for a 50μm long line, a perfect alignment required θ to be smaller than 0.00025°. It is clear that the requirement for orientation alignment is inverse proportional to the length of line. Right now in the design the smallest direction step is 0.01°, which means that the misaligned angle θ was smaller than 0.005°. In the future work, it might be necessary to adjust line length as well as direction steps to obtain good quality nanolines with feature size ~ 10 nm.

Chapter 3 Characterization and Analysis of Deformation Mechanism of SiNLs

In Chapter 3, Nano-indentation technique was used to characterize the mechanical behavior of a set of 74 nm wide SiNLs. The Nano-indentation technique was combined with finite element method (FEM) with the latter to simulate the indentation process. Material properties of SiNLs, *e.g.* elastic modulus and strain to failure, were extracted from the simulation. The metrology was also used to evaluate friction between indenter and SiNLs, and the results indicated that this approach has the potential to study friction behavior at nano-metric scale.

The first part of this chapter introduces the nano-indentation technique, describing the basic principle and its application to low-k films. It is followed by a brief introduction to buckling phenomena, since silicon nano-structures were observed to buckle under the compressive load in the indentation process. In the third part, nano-indentation experiments were performed on a set of silicon nanolines (SiNLs) of 74 nm wide, 510 nm high and with a pitch of 180 nm. A FEM model was then developed to simulate the indentation process and to evaluate material properties, including modulus, strain to failure, and friction at the contact. Finally, mechanical characterization method is summarized based on the indentation results of 74 nm wide lines.

3.1 Introduction to nano-indentation

Nano-indentation technique has been widely used to measure mechanical properties such as elastic modulus and hardness of thin films and bulk materials [97,98,99,100]. Compared with other methods such as microbeam cantilever tests or

bulge tests, nanoindentation is a convenient technique since there is no requirement for special sample preparation. Figure 3.1 shows a schematic of the nanoindentation process [101]. First, the sample surface is imaged in conventional AFM mode with a diamond indenter and positions for the indents are selected. After that, a transducer monitors and records the loading and unloading process with force and displacement measured simultaneously. A second AFM image of the surface may be used to show the shape of the indent after the indentation. Since the depth resolution is on the order of nanometers, it is possible to indent low-k thin films with sub-micron thickness. Figure 3.2 shows SEM images of three types of indenters. Typically, the Berkovich indenter is widely used in nanoindentation to extract both elastic modulus and hardness from the force vs. displacement curves. In the following, the nano-indentation technique is illustrated by using the analysis of indentation on low-k polymeric films as an example.

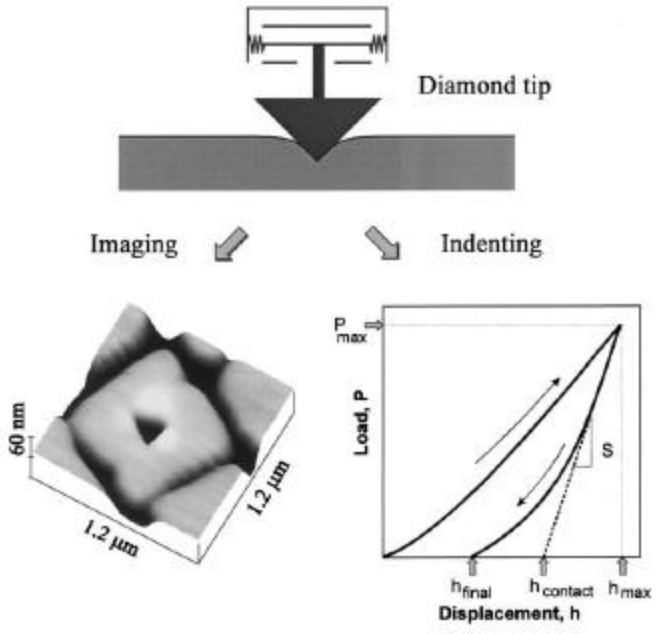
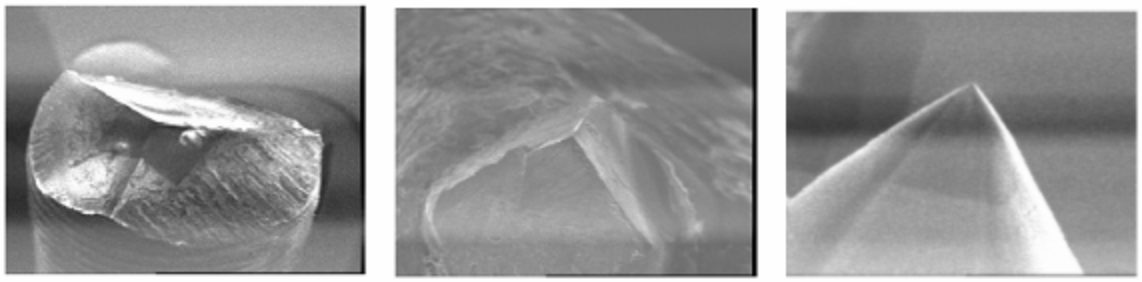


Figure 3.1 Schematic of an AFM based nano-indentation process [101].



(a) (b) (c)

Figure 3.2 SEM images of three types of indenters. (a) Berkovich indenter, 3-Sided pyramidal shape, 142.6° (edge to opposing face), and ~ 150 nm tip radius; (b) NorthStar indenter, 3-Sided pyramidal shape, Cube corner profile, and ~ 50 nm tip radius; (c) Conical indenter, conical shape, 60° included angle and > 1 μm tip radius. [Taken from Hysitron website]

In 1992, Oliver and Pharr proposed an analysis method [56], with which the elastic modulus, E, and hardness, H, can be derived directly from the analysis of the unloading force vs. displacement curve. The process is shown schematically in Figure 3.3. As the indenter is driven into a thin film, both elastic and plastic deformation occurs. The assumption of this analysis is that after the indenter is withdrawn, only the elastic displacements are recovered. The initial unloading contact stiffness S, which is determined by the slope of the unloading curve, is related to the reduced modulus (E_r) by:

$$S = \frac{dP}{dh} = \frac{2}{\sqrt{p}} E_r \sqrt{A} \tag{3.1}$$

where P is the load and h is the indentation displacement. A is the projected contact area, which is a function of displacement and could be deduced by the geometry of the indenter and the displacement h. After acquiring the contact stiffness, S, and the contact area, A, from the unloading curve, the reduced modulus E_r could be calculated from Eqs. 3.1. E_r is directly related to elastic modulus of materials and is given by

$$\frac{1}{E_r} = \frac{1-\nu_f^2}{E_f} + \frac{1-\nu_i^2}{E_i} \tag{3.2}$$

where E_f and ν_f are the elastic modulus and Poisson's ratio for the film, and E_i and ν_i are the elastic modulus and Poisson's ratio for the indenter. (For diamond tip, E_i=1141 GPa and ν_i=0.07). The hardness H of the thin film could be estimated by:

$$H = \frac{P_{max}}{A} \tag{3.3}$$

where P_{max} is the maxium load and A is the projected contact area.

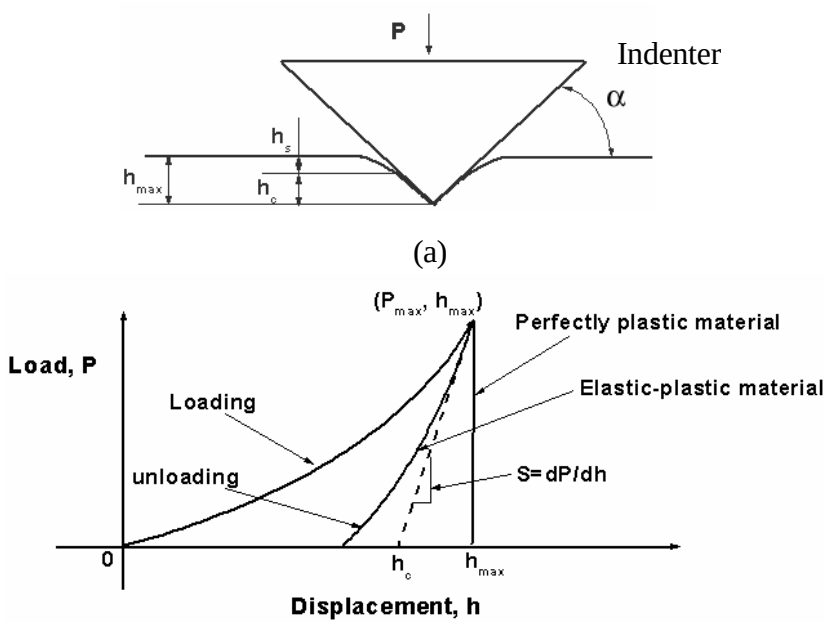


Figure 3.3 Schematic of indentation technique for modulus and hardness measurement. (a) Indentation on surface of materials; (b) typical load vs. displacement curve recorded in the indentation process.

Figure 3.4 shows a set of nano-indentation test results on a 1.5 μm thick Bisbenzocyclobutene (BCB) low-k polymer film. For the measurements, an AFM based

nanoindentation system (Triboscope by Hysitron, Inc.) was used with a Berkovich indenter with tip of radius around 150 nm. The elastic modulus and hardness were calculated according to the analysis of the unloading curves. Figure 3.4(a) shows 12 load vs. displacement curves with different peak loads. The loading curves were found to be coincident with each other. Figure 3.4(b) and (c) show the extracted reduced modulus and hardness from the 12 curves, respectively. The two data sets clearly indicated that as contact depth decreased, modulus and hardness results first decreased and then reached a plateau as the contact depth reduced to below 10% of film thickness (1.5 μm). This phenomenon was due to the influence of the silicon substrate. The Si substrate has a averaged elastic modulus of 165 GPa, which is around 50 times larger than the modulus of BCB. When the indentation depth was large, the indentation results showed a substrate effect. The effect became weaker as the indentation depth reduced. The reduced modulus and hardness of the BCB film were determined by the values at the plateau, which were around 3.7 GPa and 0.25 GPa, respectively. From Eqs. 3.2, the elastic modulus of the BCB film was calculated to be 3.3 GPa, with the assumption of a Poisson's ratio of 0.33. This value was just a little larger than that of BCB bulk, which was report to be 2.9 GPa by Dow Chemical Company. The discrepancy between these two values might be due to the substrate effect that still existed at the plateau region, although it became weaker in this region. For further de-convolution the substrate influence from indentation results might need an analytical solution [102], or the assistance from FEM simulation [103,104], which will not be discussed in this dissertation.

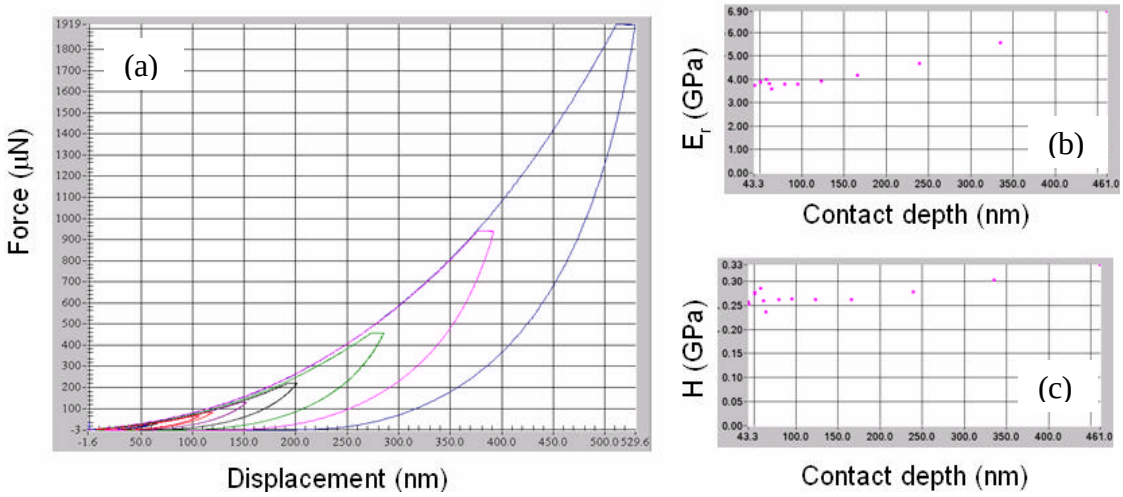


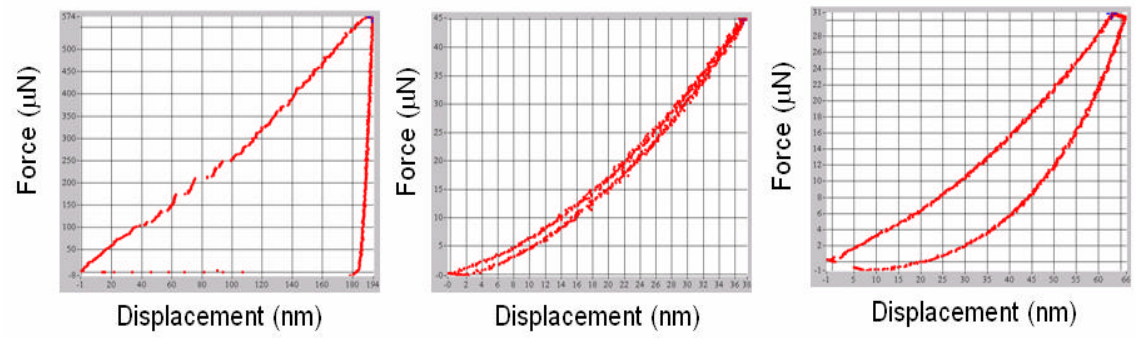
Figure 3.4 Results of nano-indentation on BCB polymer film. Film thickness is 1.5 μm. (a) Indentation force vs. displacement curves under different peak forces; (b) Reduced modulus E_r vs. contact depth; (c) Hardness vs. contact depth. The results showed the substrate effect on the extracted mechanical properties.

Figure 3.5 shows indentation responses from three different materials, including Aluminum bulk, Methyl silsesquioxane (MSQ) film and BCB film. MSQ and BCB are low-k polymers. For indentation on the two polymeric films, in order to minimize the substrate effect, the depth of contact was kept less than 10% of the film thickness in both tests. It is clear that for different materials with different mechanical properties, the indentation responses were quite different. The indentation behavior could be explained by comparing the induced strain of indentation with the yield strain of materials. The indentation induced strain could be estimated to be about $\tan\alpha$, where α is the inclination angle of the indenter to the surface (in Fig. 3.3(a), for Berkovich indenter, $\tan\alpha$ equals to ~0.3) [105,106]. And the yield stain is Y/E, where E and Y are elastic modulus and yield stress of the indented material, respectively. Thus the ratio of indentation induced strain to the yield strain of materials is proportional to:

$$\frac{\tan a}{Y/E} = (\tan a)(E/Y) \tag{3.4}$$

It was reported that, when the factor $(\tan\alpha)(E/Y)<3$, the indentation response was mainly elastic; while in the range of $3<(\tan\alpha)(E/Y)<50$, the response became elasto-plastic; and as the factor increased to beyond 50, rigid-plastic plastic deformation dominated. For aluminum (E ~ 72 GPa, Y ~ 100 MPa), thus the factor $(\tan\alpha)(E/Y)$ is beyond 200 and unrecoverable plastic deformation dominates the loading-unloading process. For a MSQ film, it is a silica-based material, which has a relatively large yield stress (~700 MPa) and a small $(\tan\alpha)(E/Y)$ (~3). Thus, the indentation response was mainly elastic, which was shown in Figure 3.5(b). For BCB, since it is a benzene based material and has a low yield stress (~50 MPa), the $(\tan\alpha)(E/Y)$ was around 20 and the indentation response was a typical elasto-plastic mode, which is shown in Figure 3.5(c). From this set of experiments, it is shown that from the force vs. displacement curves, the mechanical responses in the indentation process can be determined as a function of the indented materials.

In the next part, since buckling of SiNLs can occur during the nano-indentation process, buckling phenomena based on compression loading on column structures are briefly described.



(a) (b) (c)

Figure 3.5 Indentation responses of some materials. (a) Indentation on Al bulk, E~72 Gpa, H~0.21 GPa; (b) Indentation on MSQ film, E~7 Gpa; (c) Indentation on BCB film, E~3 GPa, H~0.25 GPa.

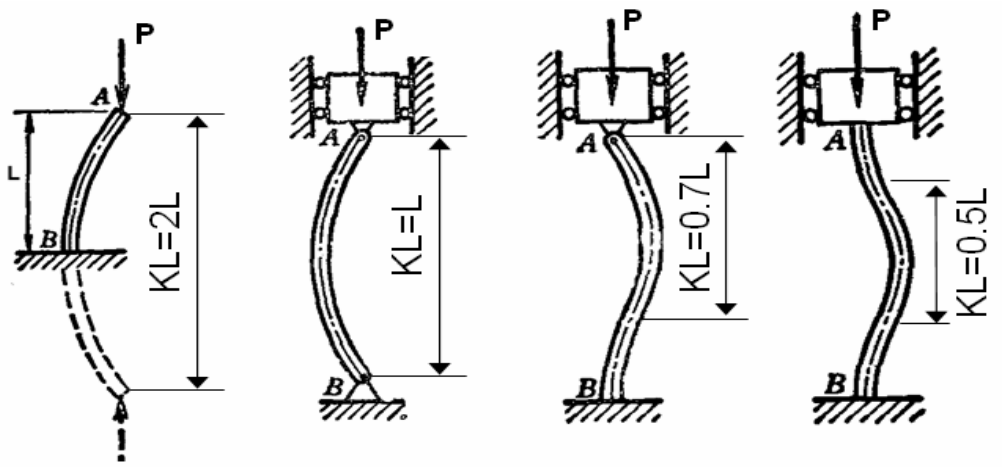
3.2 Introduction to column buckling

Buckling as an elastic instability has been observed in other nanostructures [50,107,108]. In engineering, when a structure, (*e.g.* a straight column) is loaded in compression, it may be unable to support the applied load and fail by buckling rather than by plastic deformation. The process involves the primary elastic response, followed by a sudden buckling behavior at some critical load. This failure mode is also described as failure due to an elastic instability.

In compression, a short column under an axial load will fail by direct compression instead of buckling; but, a long column loaded in the same manner will fail by buckling (or bending). The critical bucking load, which is the maximum axial load that a long column can carry without buckling, is given by the Euler formula [109]:

$$P = \frac{EIp^2}{(KL)^2} \tag{3.5}$$

where P is the maximum or critical load, E and I are elastic modulus and area moment of inertia of the column, respectfully. L is the length of column, and K is the column effective length factor, whose value depends upon the conditions of end support of the column, which is shown in Figure 3.6. For the straight column, if one end is fixed and the other end is free to move laterally, K=2.0; if both ends are pined and free to rotate, K=1.0; in the case that one end is fixed and the other end is pinned, K=0.7. In the extreme case if both ends are fixed, K=0.5. It is noted that the end conditions have a considerable effect on the critical load of the column. The boundary conditions determine the mode of bending as well as the distance between inflection points on the deflected column. For example, Mode (a) has the largest distance between the inflection points, resulting in the lowest load capacity of the column.



(a) (b) (c) (d)

Figure 3.6 Schematic of buckling of straight column under different boundary conditions [109]. (a) One end fixed and the other end free, K=2.0; (b) Both ends pined, K=1.0; (c) One end fixed and the other end pinned, K=0.7; (d) for both ends fixed, K=0.5.

Although the fabricated SiNLs are not column structures, this introduction serves to explain that the buckling behavior of nano-structures is still dependent not only on the mechanical properties and geometry of structures, but also on the boundary conditions. In the following section, nano-indentation technique was applied to measure mechanical responses of some SiNLs, to analyze their buckling behavior, and to investigate their mechanical properties.

3.3 Characterization of mechanical properties of SiNLs using Nanoindentation

In this section, the metrology used to characterize mechanical properties of SiNLs is introduced. The metrology was based on the experimental results of indentation on 74 nm wide SiNLs, and the corresponding FEM simulation for extracting material properties. Because the indentation was performed on patterned structures, the contact area in the indentation was not a continuous function of displacement and could not be evaluated according to Oliver and Pharr's method. Hence, FEM modeling was necessary for simulating the indentation process.

Figure 3.7 shows a schematically illustration of the nanoindentation on SiNLs. A conical indenter with the tip radius around 3-5 μm was used to probe the parallel SiNLs. The purpose of using such a relatively large indenter was to observe the global or collective responses of multiple SiNLs, instead of the localized deformation in one SiNLs resulting from a sharp indenter. During each indentation test, the indenter was managed to be placed directly on top of an array of parallel nanolines, filling in a 50 μm by 50 μm area of the wafer surface, by using a telescope inspecting from the sample side.

Subsequently, the indenter was brought into contact with the SiNLs, and the indentation loading and unloading process was monitored and recorded with force and displacement measured simultaneously [110]. In the indentation tests the force resolution was ≈ 0.2 μN and displacement resolution was ≈ 0.2 nm.

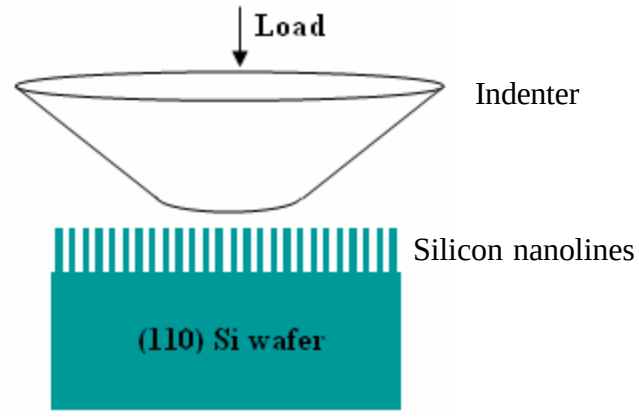


Figure 3.7 Schematic illustration of the nanoindentation experiment on silicon nanolines.

3.3.1 Experimental data of indentation on 74 nm wide SiNLs

The parallel patterned SiNLs was fabricated on a (110) silicon wafer. From the SEM images shown in Figure 3.8, the line width and the height of these SiNLs were determined to be about 74 nm and 510 nm, respectively, which corresponded to an aspect (height/linewidth) ratio of 6.9 of the rectangular cross section. The line pitch was 180 nm. In the indentation tests, the tip radius of the conical-shaped indenter was measured to be 4.6 μm, which was shown in a SEM image in Figure 3.9 . The indenter was brought into contact on the SiNLs and the applied peak load ranged from 500 μN to 1000 μN.

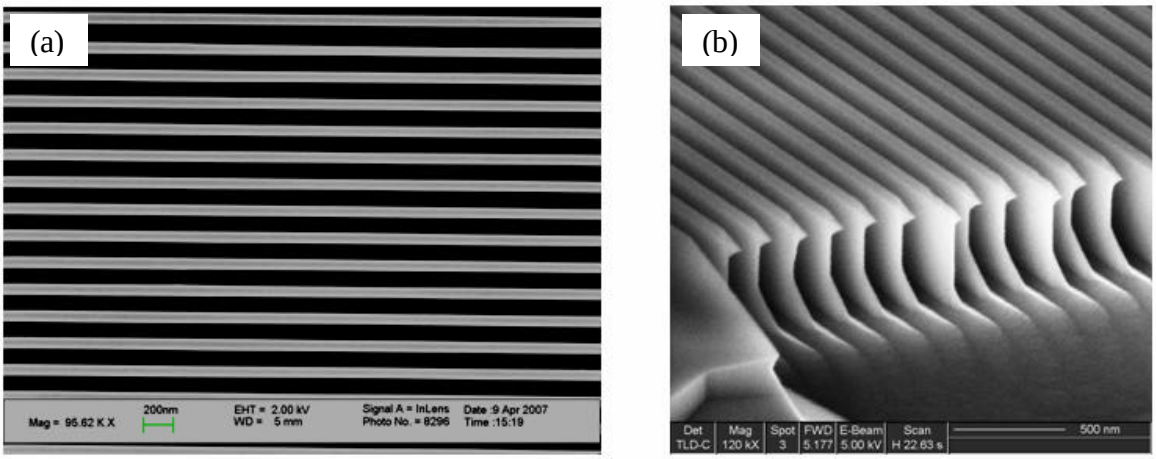


Figure 3.8 SEM images of the parallel silicon nanolines, with 74 nm line width and 510 nm height. The line pitch is 180 nm. (a) Plan view; (b) Cross-sectional view with 60° tilt angle. A small trench pattern is specially designed at one end of the line to facilitate the cross-sectional SEM imaging, showing the sharp edges due to the anisotropic etching.

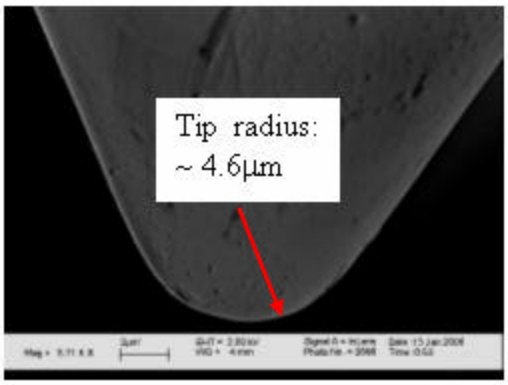


Figure 3.9 An SEM image of the conical-shaped indenter with the tip radius ~ 4.6 μm.

Figure 3.10 shows a set of force-displacement curves obtained from the nano-indentation tests on the 74 nm SiNLs. For the first test (Curve i in Figure 3.10(a)), a small indentation load of 500 μN was applied and subsequently unloaded, which exhibited an elastic response with the loading and unloading curves coinciding. With the indentation load increased to ~ 550 μN and beyond, a large displacement burst without load increase

was observed. This indicates the occurrence of an instability of the SiNLs under indentation. Interestingly, the displacement burst was fully recovered without residual deformation after the withdrawal of the indenter, which is shown in Figure 3.10(a) for the second and third tests (Curves ii and iii). Additional indentation tests with the SiNLs, which are shown in Figure 3.10(b), showed irrecoverable residual deformation after unloading of the indenter.

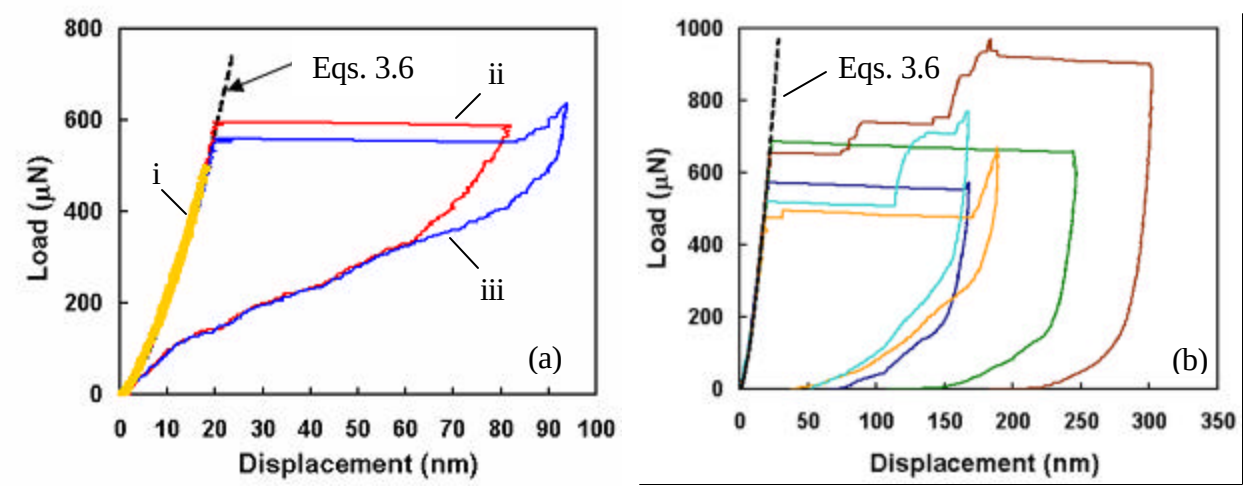


Figure 3.10 Load vs. displacement curves of a set of nanoindentation tests of parallel SiNLs with 74 nm line width and 510 nm height. (a) For the three indentation tests (Curves i, ii and iii), no residual deformation was observed after withdrawal of the indenter. (b) Load vs. displacement curves from 5 indentation tests. Fracture of the SiNLs led to large residual displacement after unloading of the indenter. The dark dash line represents the theoretically predicted elastic response by Eqs. 3.6 using an effective modulus $E^* = 72$ GPa.

.

Similar displacement bursts were observed in nanoindentation experiments of metal films, which were attributed to a dislocation mechanism as an intrinsic material instability [60]. Here, however, the magnitude of the displacement burst was much larger (over 60 nm in comparison with a few nanometers for the metal films). As noted in a

previous study [42], plastic deformation of nanoscale single-crystal Si beams was observed only at elevated temperatures (>373 K); thus, the dislocation mechanism was not expected to operate at the room temperature. Furthermore, after some displacement bursts the displacement was fully recovered upon unloading of the indenter as shown in Figure 3.10(a). This suggests that the material remained elastic before and after the displacement burst, where the instability was most likely due to buckling of the SiNLs. In particular, the observation of this full displacement recovery of the parallel SiNLs after buckling is similar to the reported supercompressible behavior of foam-like carbon nanotube (CNT) films [108]. The latter was attributed to a cooperative buckling mechanism of the vertically aligned carbon nanotubes (VACNTs).

As the peak load increased, irrecoverable residual deformation was left after unloading as shown in Figure 3.10(b). The maximum indentation displacement for each test in Figure 3.10(b) was greater than 150 nm, while in Figure 3.10(a) the maximum displacement was less than 100 nm. The larger indentation displacement implied more significant bending of the SiNLs after the buckling instability, which in turn induced higher tensile stresses that eventually fractured the SiNLs. Figure 3.11(a) shows the SEM image of the SiNLs after fracture. The debris of the fractured SiNLs were of isosceles triangular shape in the (111) crystalline plane parallel to the SiNLs, with two sides in <110> directions and the base side in the <112> direction of the SiNLs. As shown by the schematic drawing in Figure 3.11(b), the two side planes of the triangular debris were formed as a result of fracture along the $(\bar{1}\bar{1}1)$ and $(1\bar{1}1)$ crystalline planes, indicating a primary cleavage mechanism of the close packed {111} planes along the <110>

directions [57]. The triangular shape is also a reflection of the buckling-induced tensile stress distribution in the SiNLs, which intensified along the bending ridges of the nanolines under the indenter.

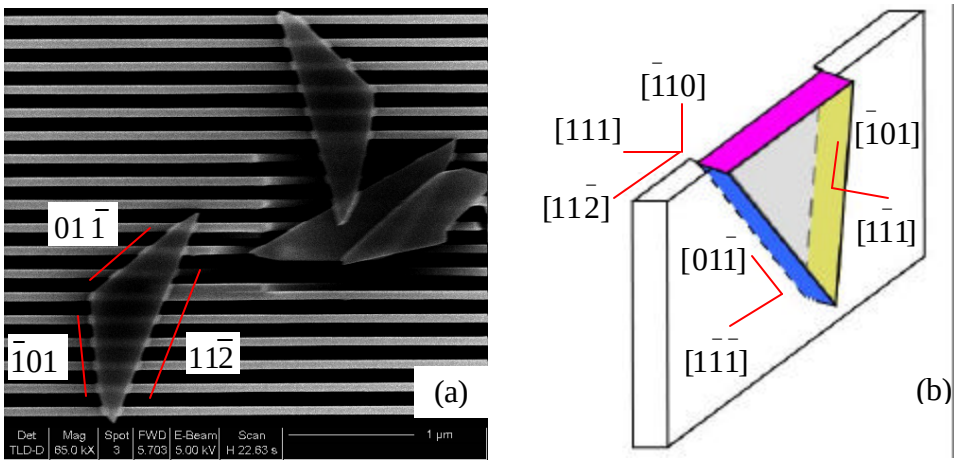


Figure 3.11 (a) An SEM image of the fractured nanolines after one indentation test. The fracture debris are of isosceles triangular shape in the (111) crystalline plane, indicating a cleavage fracture mechanism; (b) Schematic illustration of the crystalline orientations for the Si nanolines and the cleavage planes in the formation of the triangular fracture debris. The two side planes of the debris were formed as a result of fracture along the $(1\bar{1}\bar{1})$ and $(\bar{1}\bar{1}1)$ crystalline planes.

3.3.2 Application of Hertz theory on the indentation elastic response

As a starting point for the analysis of load vs. displacement curves, the elastic response in the indentation was stuied. The well-known Hertz theory of contact mechanics for a spherical indenter onto a planar surface was employed [56]. It predicts a force-displacement relationship in the elastic region as follows:

$$P = \frac{4}{3} E^* h^{3/2} R^{1/2} \tag{3.6}$$

where P is the indentation load (force), h is the indentation depth (displacement), R is the radius of the spherical indenter, and E^* is the effective modulus depending on the moduli of the indented material and the indenter, i.e.,

$$\frac{1}{E^*} = \frac{1-\nu_1^2}{E_1} + \frac{1-\nu_2^2}{E_2} \tag{3.7}$$

where ν is Poisson's ratio, and the subscripts 1 and 2 refer to the two materials. For the present study, these refer to Si and diamond, respectively. For diamond indenter, E_2 and ν_2 are 1140 GPa and 0.07, respectively. It is found that the initial portion of the load-displacement curves in Figure 3.10 could be well fitted by Eqs. 3.6 with an effective modulus of E^* = 72 GPa. This value was significantly lower than the effective modulus for indentation on a planar surface of bulk Si, which is 153 GPa according to Eqs. 3.7. (The averaged elastic modulus and the Poisson's ratio of Si are 163 GPa and 0.27, respectively). As would be expected, the nanoscale patterning effectively reduced the stiffness of the Si surface under indentation. Since the tip radius of the indenter (~4.6 μm) was much larger than the pitch of the SiNLs (180 nm), there was not enough lateral resolution in the indentation system to identify the exact location of the indenter tip relative to the individual SiNLs, which could vary from a trench center to a line center of the parallel pattern. Nevertheless, it is noted from Figure 3.10 that the initial elastic response (before the displacement burst) of the SiNLs was reproducible, thus insensitive to the relative location of the indenter tip. This behavior was similar to the response of a film-like material. The deviation from the initial elastic response occurred with a displacement burst at a critical load in the range of 480 μN to700 μN (see Figure 3.10).

This has been attributed to a buckling instability of the SiNLs. In the next part, a 3D FEM simulation was developed for further interpreting the indentation results.

3.3.3 FEM simulation of indentation on SiNLs

FEM is widely used for the simulation analysis of experimental results for the study of material properties under indentation [60,99, 111]. Generally speaking, the unknown material properties are determined by first using them as input parameters in FEM until best fit to the experimental load vs. displacement curves is obtained. Then the indentation process details could be examined accordingly. As shown in Figure 3.12, a spherical indenter on twelve parallel lines was modeled using the commercial FEM package ABAQUS [112]. The tip of the indenter was located at the trench center. It was found that adding more lines did not change the simulation results for the initial elastic response and the critical load. Since the modulus of the diamond tip (1140 GPa) was much higher than the modulus of Si (163 GPa), the indenter was modeled as a rigid body. Under this assumption, the modulus of silicon (E_1) used in the model came out somewhat different from its bulk value. The extraction of E_1 was based on the fact that the effective modulus of the contact should be the same under the conditions of with and without the rigid body assumption. Then according to Eqs. 3.7,

$$E_1 = E^* * (1 - n^2) = 153 * (1 - 0.27^2) = 144 GPa \quad (3.8)$$

Here three kinds of Si modulus have been defined. The averaged elastic modulus was 163 GPa, and the plain strain or effective modulus of bulk Si under diamond indentation was

153 GPa. In FEM, under the condition of rigid body indenter assumption, the elastic modulus (E_1) used was around 144 GPa.

In simulation, the Si lines were supported at the bottom by a rigid substrate as an approximation for the un-etched part of the Si wafer. It was found that modeling with an elastic substrate significantly increased the computational time but gave a slightly lower critical load. In simulation, a vertical displacement was applied to the reference node of the indenter until the maximum indentation depth was reached. The indentation force was obtained by the reaction force at the reference node of the rigid body. The contact between the tip and the lines was initially assumed to be frictionless.

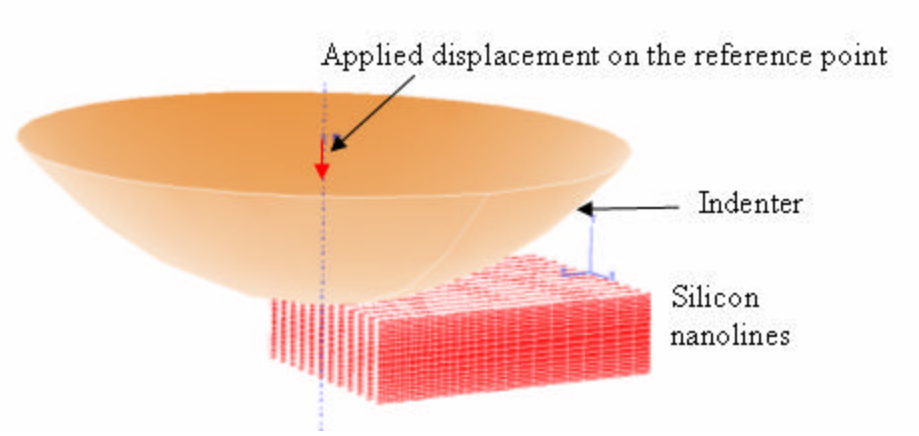


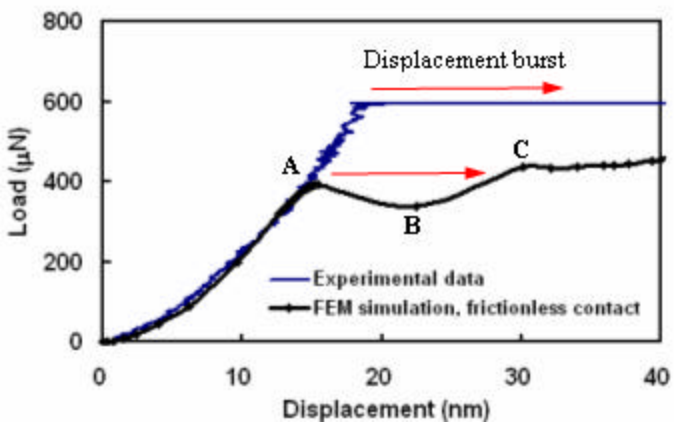
Figure 3.12 Layout of the 3D FEM model of indentation on silicon nanolines.

Figure 3.13 shows the FEM simulation result when the indenter was located at the pattern trench center. Although elastic modulus of bulk silicon was adopted in the simulation, the simulation curve matched well the experimental data in the elastic region. This indicates that the elastic modulus of Si remained unchanged for nanolines with feature size down to 74 nm. The elastic properties of the SiNLs used in this FEM

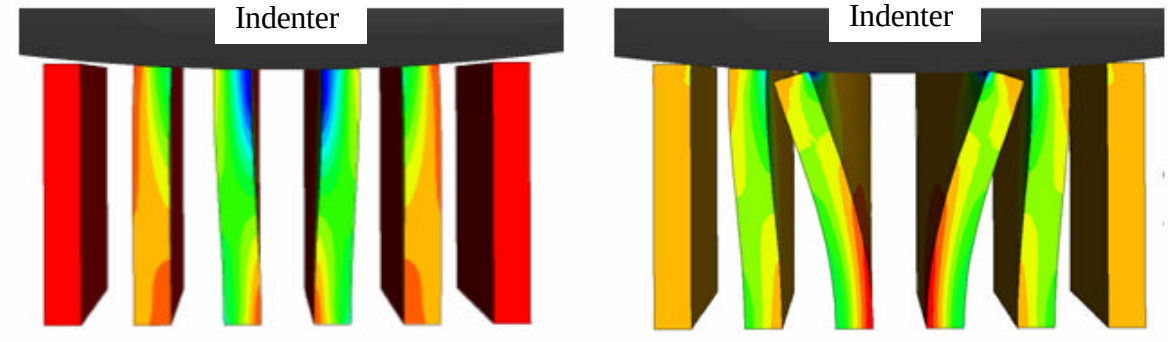
simulation were: Young's modulus E = 140 GPa and Poisson's ratio ? = 0.27. This modulus is slightly smaller than the calculated modulus (E_1) of Si (144 GPa). Since previous studies of Si beams [41] and SiNWs [46] showed no size effect in the elastic modulus of Si, the discrepancy was mainly attributed to the approximations in the numerical model that assumed a rigid substrate and isotropic elastic properties.

At a critical load (marked as A in Figure 3.13(a)), the simulation predicted a drop of the indentation load under the displacement control. This is an indication of softening of the nanolines under the indentation, which would lead to a displacement burst during a load-control experiment. The critical load for the displacement burst can be determined from the first peak of the simulated curve. Figure 3.13(b) and (c) show the simulated deformation of the nanolines immediately before and after the critical load, from which a transition of the buckling mode was observed. Below the critical load, the two center lines were bent symmetrically into a half-wave mode with the top nearly perpendicular to the surface of the indenter. After the critical load, the lines were bent into a quarter-wave mode, which was structurally softer than the half-wave mode. Such a transition led to the drop of the indentation load (from A to B) under the displacement control; or equivalently, a displacement burst (from A to C) under the load control. It is noted that the magnitude of the displacement burst predicted by the static simulation was much smaller than that observed in experiments. This might be addressed with a more accurate model that takes into account the dynamic postbuckling behavior. Nevertheless, the present model was sufficient for the simulation of the initial elastic response and the prediction of the critical load. It may be pointed out that the transition of buckling mode

was a rather unique behavior, owing to the high aspect ratio and nearly perfect rectangular cross sections of the nanolines.



(a)



(b) (c)

Figure 3.13 FEM simulation of the silicon nanolines under indentation. The tip of the indenter is located on top of the trench center of the 74 nm silicon nanolines. (a) plots of the simulated load-displacement curve and loading part of one set of indentation data (Curve ii in Fig. 3.10(a)), showing coincidence of elastic response. At the critical load (marked as A), the simulation predicts a drop in force from A to B due to the transition of the buckling mode. Under a load-control experiment, the simulation predicts a displacement burst from A to C. (b) and (c) show the deformation of SiNLs before and after the mode transition at the critical load, corresponding to A and B marked in (a), respectively. Since the indentation displacement was small, only deformations of 6 lines are included in these plots.

It is found that the critical load as predicted by the numerical model depended on the relative location of the indenter tip on top of the nanolines and the friction at the

contact between the Si lines and the indenter. The relative location of the indenter was varied from the trench center to the line center of one side in the simulations. It was found that the relative location had insignificant influence on the initial elastic response, confirming the film-like behavior under a relatively large indenter. On the other hand, without friction the critical load increased significantly when the indenter was located on the line center. Figure 3.14 shows the deformation of SiNLs as indenter was put on line center in the FEM simulation. The center line was under compression and did not buckle. The displacement burst in the indentation was from buckling of the side lines, leading to an increase of the critical load compared with the case of indenter placed on trench center. This might be responsible for the scatter of the critical loads from the indentation tests as there was not enough lateral resolution to identify the exact location of the indenter.

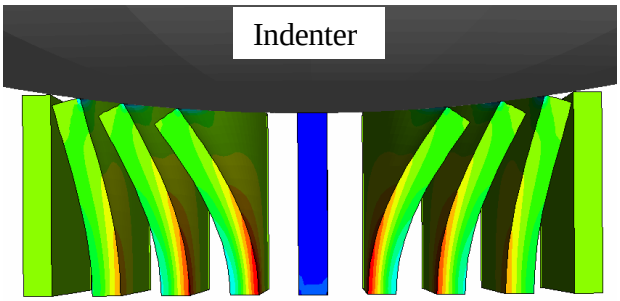


Figure 3.14 FEM simulation of the silicon nanolines under indentation. The tip of the indenter is located on top of the line center of the 74 nm silicon nanolines. It is shown that the center line was under compression and did not buckle. The displacement burst in the indentation was from buckling of the side lines.

The friction at the nanoscale contact is of fundamental interest [113,114]. Here, by using a simple Coulomb friction model, it was found that the critical load increased as the friction constant at the contact increased. On the other hand, the frictional contact

property did not influence the initial elastic response under indentation. Figure 3.15 plots the predicted critical load as a function of the friction constant, with the indenter located at the trench center and the line center, respectively. This provided the lower and upper bounds of critical buckling loads corresponding to each friction coefficient. Without friction, the Si lines slided freely along the surface of the indenter. With friction, the sliding of Si lines was suppressed, leading to a delay of transition of the buckling mode as well as a higher critical load. When the indenter tip was at the trench center and the friction coefficient increased to beyond 0.012, there was a sudden jump of the critical load. This jump was due to the fact that the friction force increased to a level that the movement of Si lines was confined to indenter surface. The confinement resulted in a structure failure mode transition from line bending outwards to line bending inwards, which corresponded to mode (a) and mode (c) in Figure 3.6, respectively. The phenomenon will be further discussed in the next Chapter.

The critical load thus offers an indirect measure of the friction at the nanoscale contact. Taking 480 μN as the lower bound for the critical load (see Figure 3.10(b)), the friction coefficient at the contact was estimated to be about 0.01. This value was about one order of magnitude lower than those obtained from a tribological test using a spherical diamond tip (tip radius 20 μm) on single-crystal Si (100) wafers [115]. The present study suggests that the effect of contact friction may also be important in other nanomechanical tests such as the AFM bending tests of nanowires and nanobelts.

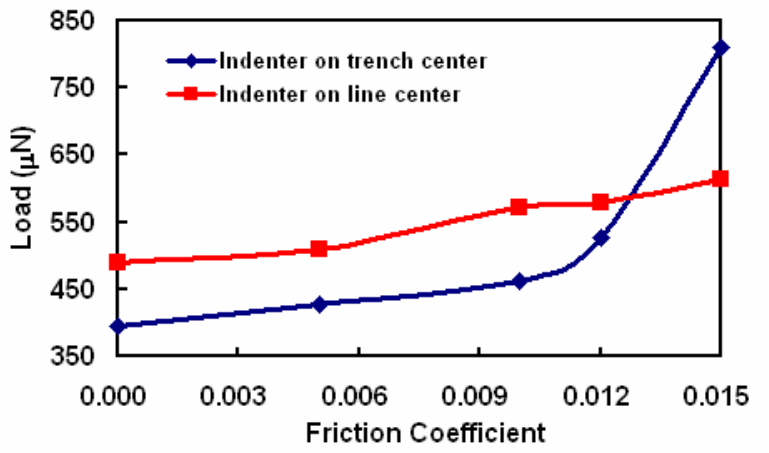


Figure 3.15 The critical indentation load predicted by the finite element model, as a function of the friction coefficient between the indenter tip and the Si nanolines. The two lines are for the tip located at the trench center and the line center, respectively, as the lower and upper bounds for the critical load.

To estimate the critical strain to fracture, a finite element simulation was conducted up to 90 nm indentation depth as shown in Figure 3.16, from which a maximum principal strain of 8.5% was obtained at the bottom ends of the two central lines. Although the present model was not accurate for the postbuckling analysis, the bending strain as a geometric measure serves as a reasonable estimate for the deformation of the SiNLs. Since the SiNLs did not fracture up to a 90 nm indentation depth as shown in Figure 3.10(a), the strain to fracture for the SiNLs was estimated to be above 8.5%. This strain is comparable to those reported by Hoffmann et al. [15] for SiNWs, but still significantly lower than the theoretical critical strain (17%) [45] for Si under tension in the <111> direction. The high crystalline quality and surface smoothness of the nanolines are critical for the observation of cleavage fracture of Si at the nanoscale (See Figure 3.11), as the fracture process is highly sensitive to the surface defects.

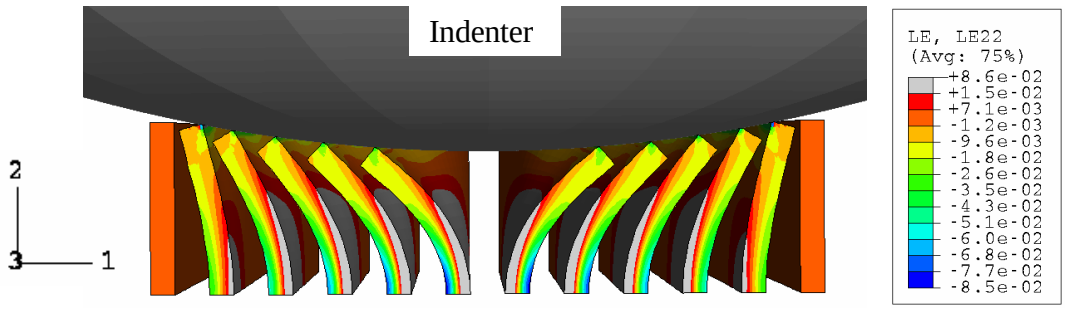


Figure 3.16 FEM simulation shows the deformation of the nanolines with 90 nm indentation displacement indentation on SiNLs. Indenter was located on trench center. As an estimation of the strain to fracture, the maximum principal strain was ~ 8.5%, which was at the bottom end of the two central lines.

3.4 Summary

Single-crystal Si nanolines was fabricated with 74 nm linewidth and an aspect ratio around 6.9. The Si nanolines had nearly atomically flat sidewalls with almost perfectly rectangular cross sections and highly uniform linewidth. Using an atomic force microscope (AFM) based nanoindentation system, the elastic, fracture, and friction properties of the Si nanolines were characterized. A buckling instability was observed at a critical load, with fully recoverable deformation after a displacement burst. A finite element model was developed to simulate the elastic response and to predict the critical load. It was found that the critical load for buckling instability was sensitive to the friction coefficient at the contact. With larger indentation displacements, irrecoverable displacements were observed due to fracture of Si nanolines, with the strain to failure estimated to be above 8.5%. The fracture debris were of isosceles triangular shape along specific crystalline orientations, indicating a cleavage fracture mechanism under the effect of buckling induced stress distribution. This study demonstrates a valuable

approach for nanoscale mechanical characterization using the well-defined nanoline structures and the nanoindentation method.

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Chapter 4 Geometry Effect on the Deformation Behavior of SiNLs

In Chapter 4, the deformation behavior of two sets of SiNLs, with a similar aspect ratio as high as 16 and feature size scaled down to 24 nm, was characterized by nanoindentation technique and corresponding FEM simulation. For a better control in indentation, trench width of these SiNLs was widened to be larger than 360 nm. This enabled the positioning of the indenter on the pattern trench center by an AFM scanning before indentation. It was found that the buckling behavior of these SiNLs were dependent on the combination effects of load, line geometry, mechanical properties of SiNLs, and the friction properties at contact. The results will be discussed in this chapter.

The first part of this chapter is an introduction to the indentation conditions, including dimensions of the indented SiNLs, locating the indenter on the SiNLs, etc. Then nanoindentation results of the two sets of SiNLs (having a similar AR of ~ 16) were presented, showing that the deformation behavior was directly related to the line geometry and the friction at contact. Finally, the results of the mechanical study are summarized.

4.1 Geometry of indented SiNLs

Table 4.1 shows the dimensions of the two sets of SiNLs fabricated for investigation of the geometry effect on deformation behavior under nanoindentation. In the SiNL set 1, the line height was 380 nm, corresponding to a wet etching time of ~ 20 seconds. For the SiNL set 2, the etching time was ~ 1 minute and the line height was

about 1.4 μm. The feature sizes of the two nanoline sets were 24 nm and 90 nm, respectively, resulting in a trench width of ~360 nm in both sets of nanolines. The aspect ratio of the nanolines was around 16. The variation of line dimensions enabled the study of geometry effect on deformation behavior as well as mechanical properties of SiNLs at the nanometer scale.

Table 4.1 Dimensions of SiNLs fabricated for indentation tests.

Line Dimension (nm)	SiNL set 1	SiNL set 2
Width	24	90
Height	380	1400
Pitch	390	450
Trench width	366	360
Aspect ratio	15.8	15.6

In Chapter 3, the pitch of the 74 nm wide line was 180 nm, indicating a trench width of ~ 106 nm. In this case, the lateral resolution was not enough to identify the exact location of indenter tip during nanoindentation experiments. In order to improve the indentation control, the pitch of SiNLs was designed to be larger than 390 nm, resulting in a larger trench width of nanolines (>360 nm in Table 4.1). Figure 4.1 shows an AFM image of SiNLs scanned by the conical indenter before indentation. The AFM image was a convolution of the SiNL dimension and the tip radius of the indenter (~ 4 μm), leading to an apparent widened linewidth and a narrowed trench gap in the image. In this situation it was more accurate to locate the indenter on the trench center than on the line

center. Hence, in the following tests, the indenter was positioned on the trench center of the SiNLs before indentation, which was indicated by the white cross in Figure 4.1.

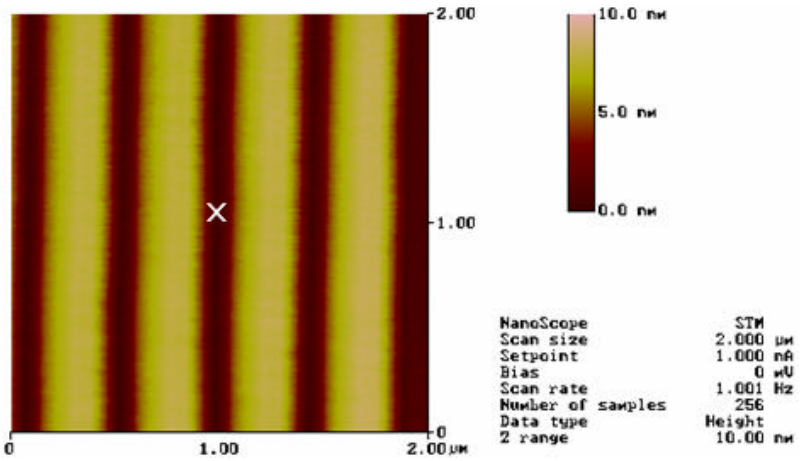
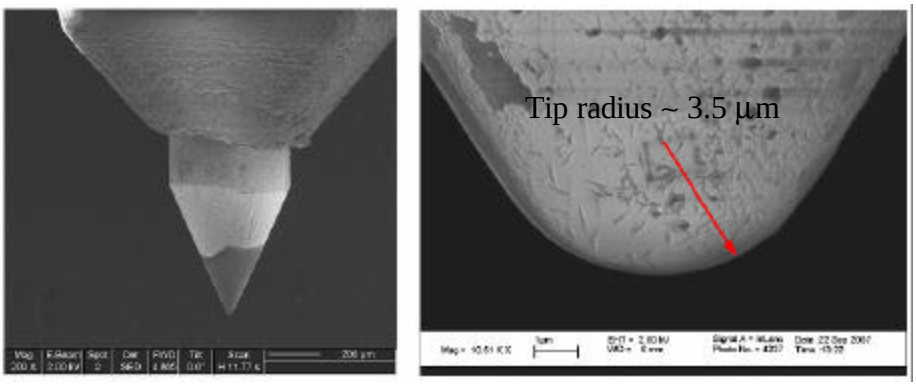


Figure 4.1 Before indentation the SiNLs were imaged in conventional AFM mode with the conical indenter. Since the image was a convolution of the large indenter and dimension of the SiNLs, the linewidths were apparently wider than their real dimension. The indenter was then located on trench center of SiNLs, which was indicated by the white cross in the image.

Since the previous indenter was broken, a new conical indenter was used in the following measurements. Figure 4.2 shows SEM images of the conical-shaped indenter. The tip of radius was determined to be 3.5 µm. In the indentation, the indenter was first located on the trench center, and then brought into contact on the SiNLs. Load-controlled indentations were performed with a trapezoidal-loading profile having a dwell time of 1s at the peak load. Because the indenter could be located on the trench center, the SiNLs was no longer film-like. Thus the Hertz's model would not be used for data analysis. Since these two sets of nanolines had a similar AR, it is interesting to compare their indentation responses and to investigate their deformation behavior. The results will be presented in the following section.



(a) (b)

Figure 4.2 SEM images of the new conical-shaped indenter with the tip radius ~ 3.5 µm. (a) overview of the nanoindenter; (b) High magnification SEM image of tip of indenter.

4.2 Nanoindentation on 24 nm wide SiNLs

Figure 4.3 shows plan-view and cross-sectional SEM images of the SiNL set 1. The line width and the height of these SiNLs were about 24 nm and 380 nm, respectively. The AR was 15 and the line pitch was 390 nm. Some hillocks appeared on SiNLs, which may due to a fast wet etching in the fabrication process.

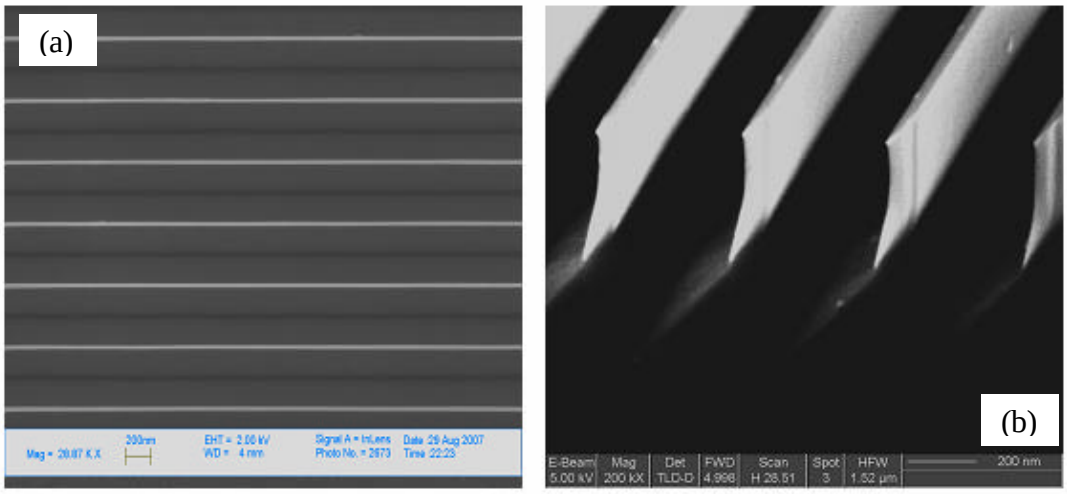


Figure 4.3 SEM images of the 24 nm SiNLs (a) Plan view; (b) Cross-sectional view with 60° tilt angle.

4.2.1 Experimental data

Figure 4.4 shows two sets of force-displacement curves obtained from the nano-indentation tests. Similar to the indentation response of 74 nm wide SiNLs, a displacement burst was observed at a critical load, which was due to the buckling of SiNLs. In these tests the displacement were fully recovered and no residual deformation left after withdrawal of the indenter. Two different deformation modes are observed in Figure 4.4. In Deformation Mode I as shown in Figure 4.4(a), for these 7 indentation tests the critical load ranged from 9 μN to 17 μN. The displacement of indenter was increased to ~ 220 nm under a ~ 70 μN force. However, in Deformation Mode II (See Figure 4.4(b)), the critical loads jumped into a range of 24 μN to 30 μN. And under the same 70 μN force the displacement was only around 80 nm, showing a much higher averaged stiffness compared with that of the deformation mode in Figure 4.4(a). For each set of the indentation tests, the unloading curves coincided well with each other, indicating a good repeatability in the experiments. Since the indentation tests were performed on the same set of SiNLs at different locations, these different deformation modes were most likely attributed to the distribution of local friction properties at each indentation contact. To initiate the data analysis, the focus was first placed on the explanation of Deformation Mode I in Figure 4.4(a). After investigating the friction influence on the indentation responses, the mechanism of Deformation Mode II was introduced.

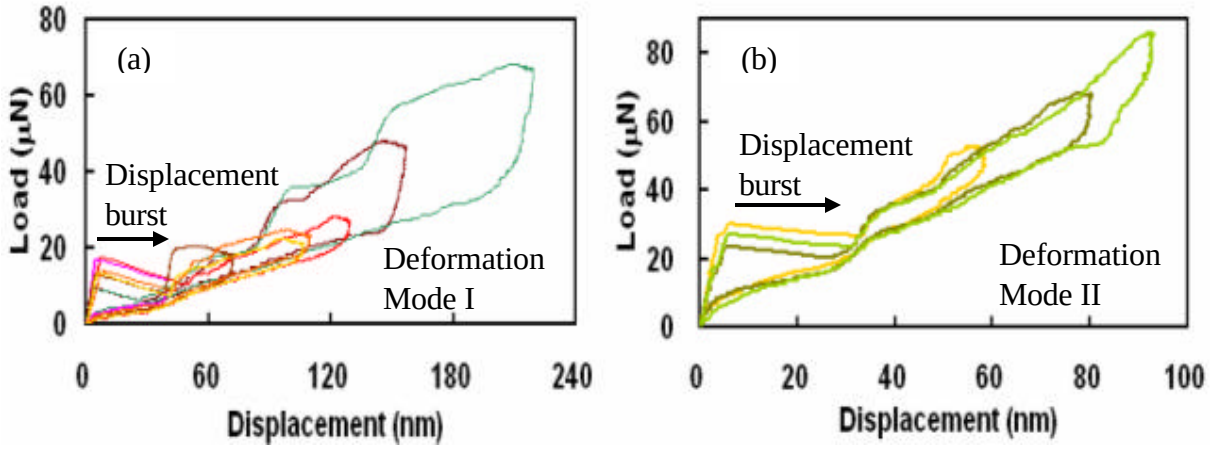
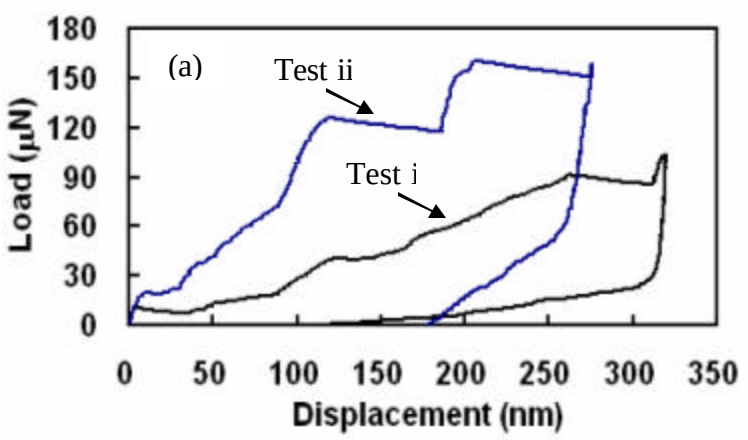
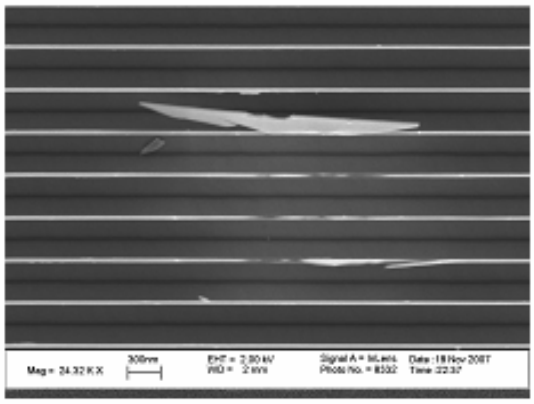


Figure 4.4 Load vs. displacement curves of two sets of nanoindentation tests of the 24 nm wide SiNLs. Indenter was positioned on the trench center of the SiNLs. No residual deformation was observed after withdrawal of the indenter. Two different deformation modes were observed: (a) Deformation Mode 1: for these 5 indentation tests, critical load ranged from 9 μN to 17 μN. (b) Deformation Mode 2: for these 3 tests, critical load ranged from 24 μN to 30 μN. The stiffness of unloading process was much higher than that of Deformation Mode 1.

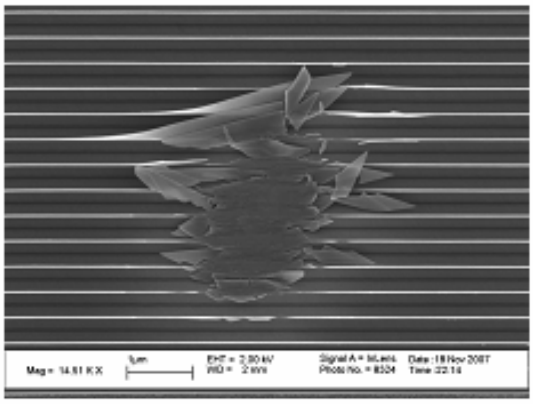
In Figure 4.4(a) before buckling of the SiNLs, the elastic responses of these indentation tests coincided with each other, following a similar loading path. For this set of SiNLs, owing to their narrow linewidth and high AR, the critical buckling loads ranged from 9 μN to 17 μN, which were much smaller than those of indentation on 74 nm wide lines in Chapter 3 (480 μN- 700 μN). The maximum indentation displacement for each test was as high as 220 nm. This was about 58% of the line height, which indicated the occurrence of a large magnitude of bending in the indentation.

As the peak load further increased, an irrecoverable residual deformation was observed after unloading, which was due to fracture of SiNLs as shown in Figure 4.5.





(b)



(c)

Figure 4.5 Fracture of the SiNLs led to large residual displacement after unloading of the indenter. (a) Load vs. displacement curves of two indentation tests. (b) and (c) are two SEM images of the fracture SiNLs after indentation Test i and indentation Test ii, respectively.

In Figure 4.5(a) the two indentation curves, Test i and Test ii, represented fracture behaviors of the SiNLs observed. These two curves correspond to the extension of Deformation Mode I and Deformation Mode II under higher loads, respectively. The maximum displacement of Test ii was ~ 270 nm, which was smaller than that of Test i (~ 320 nm). The SEM images of the fracture SiNLs after indentation Test i and Test ii are shown in Figure 4.5(b) and Figure 4.5(c), respectively. Interestingly, it was found that in

Figure 4.5(c) at the center of the indent the SiNLs were crushed to become mud-like pieces, which was quite different from the fracture observed in the indent in Figure 4.5(b). The difference between the two indents suggests that the fracture mode may be attributed to different deformation behaviors under indentation.

It is noted in Figure 4.4 that there was a load drop going through the displacement burst. This phenomenon was due to an open-loop feedback control in the indentation system. In the indentation, a small portion of the load might be absorbed by the springs of the transducer, leading to a drop of load particularly for indentation on soft materials. This issue may be solved by upgrading the feedback control from open-loop to close-loop in the future.

4.2.2 FEM simulation results

FEM analysis was employed to simulate the indentation processes and to extract mechanical properties of the SiNLs. The model was similar to that described in Chapter 3. In the model, the indenter and the silicon substrate underneath the SiNLs were both assumed to be rigid body as an approximation. The indenter was located on pattern trench center, simulating the experimental setup. In simulation, a vertical displacement was applied to the reference node of the indenter and the indentation force was obtained by the reaction force at the reference node. The friction at the contact of the indenter and the SiNLs was simulated by a simple Coulomb friction model. The friction coefficient in FEM changed from 0, for a frictionless contact, to 0.05 to investigate the influence of friction on indentation responses.

Figure 4.6 shows the FEM simulation results with variation of the friction coefficient μ. In Figure 4.6(a), μ changed from 0 to 0.05. The simulated load vs. displacement curves showed a coincidence of the elastic loading part. This indicated insensitivity of the initial elastic responses to the friction at the contact. The simulation curves predicted a force drop after a critical load, which corresponded to a displacement burst under a load-controlled experiment. The calculated critical buckling load increased from 7 μN to 29 μN as friction coefficient μ increased from 0 to 0.05, indicating more confinement on the sliding of SiNLs along indenter surface as the friction force increased. The function of friction here was like a force barrier to prevent the SiNLs from buckling into a quarter wave mode.

Figure 4.6(b), (c) and (d) include comparisons between the simulated load-displacement curves with friction coefficient μ changed from 0.02 to 0.05 and the corresponding indentation data. In Figure 4.6(b) and Figure 4.6(c), the friction coefficient was 0.02 and 0.03, respectively. The simulation curves matched well with experimental data in the elastic region. Since the elastic modulus used in the simulation was that of bulk silicon, this indicated that the elastic modulus of Si nanolines remained the same as bulk silicon with feature size down to 24 nm. It is noted that in Figure 4.6(d) that there was a discrepancy in the elastic loading part. This might be attributed to a small sliding of the top of SiNLs on the indenter surface, since in the reality, the contact condition was not as uniform as in the simulation.

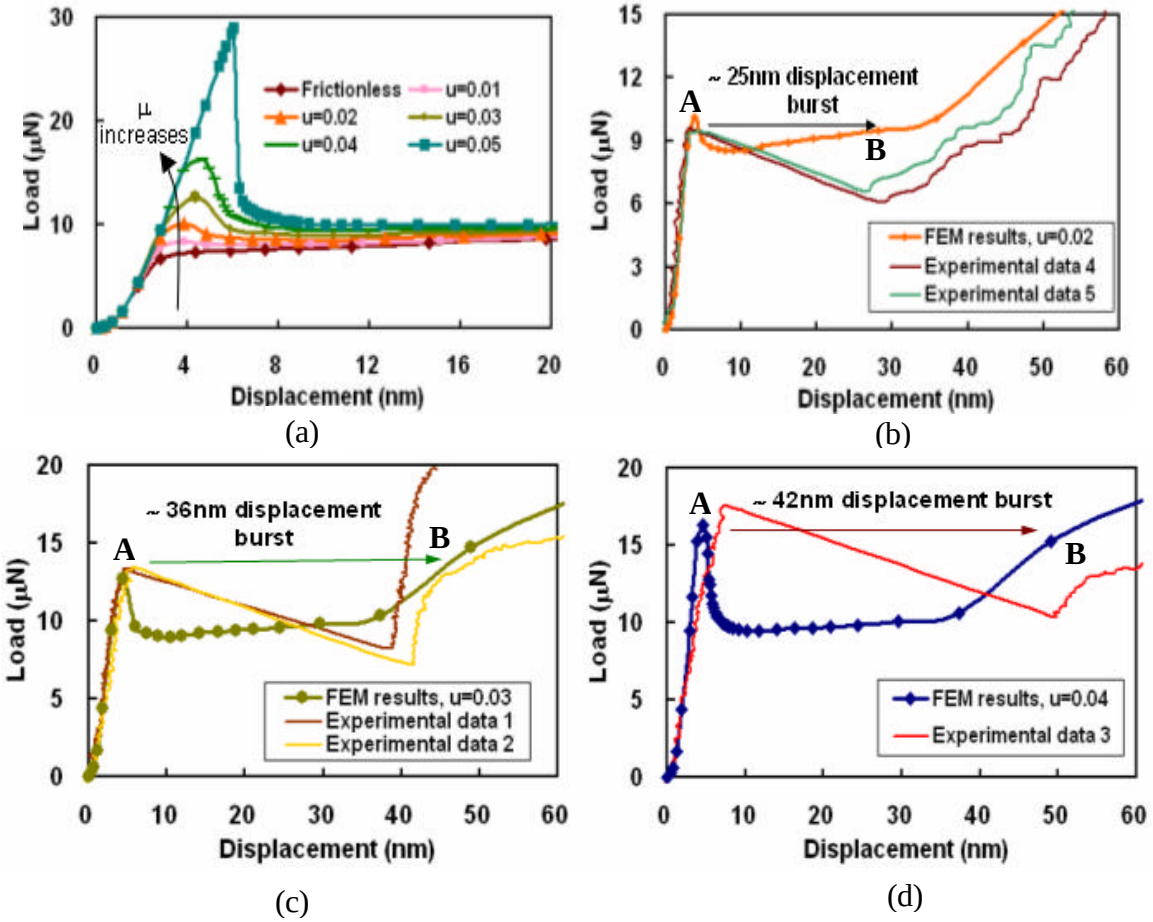


Figure 4.6 FEM simulation of the 24 nm wide SiNLs under indentation. The indenter was located on top of the trench center. (a) plots of the simulated load-displacement curves. The maximum displacement was 20 nm. Friction coefficient μ changed from 0 to 0.05, showing increase of critical load as μ increased. (b), (c) and (d): comparisons between the simulated load-displacement curves with various μ and the corresponding indentation data. The maximum displacement was 60 nm for these three pictures. The simulated curves were in good agreement with experimental data in the elastic responses. Meanwhile, the model predicted the critical load and the magnitude of displacement burst under various μ, which matched well with some indentation data shown in Figure 4.4(a).

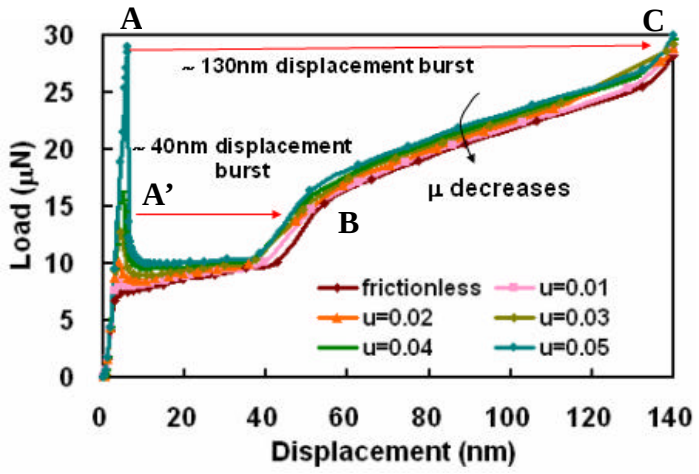
In Figure 4.6(b) with a friction coefficient μ of 0.02, the simulated indentation curve predicted a critical buckling load of 10 μN (marked as A on the peak load). And a ~25 nm displacement burst in load-controlled indentation experiment was obtained (from

A to B), which was consistent with the two sets of experimental data as shown Figure 4.6(b). Table 4.2 lists some predicted critical loads and the magnitude of displacement burst by FEM simulation as friction coefficient varied. These results matched well with experimental data as indicated in Figure 4.6(c) and Figure 4.6(d).

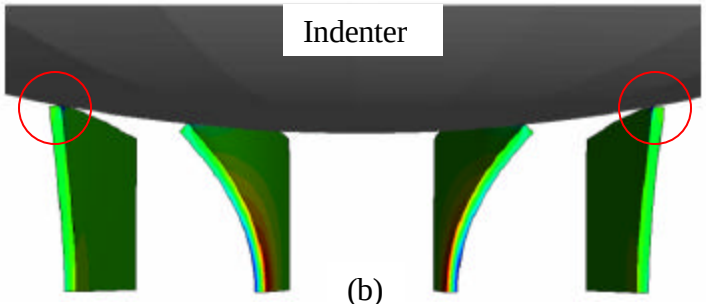
Table 4.2 Estimated critical loads and the magnitude of displacement burst by FEM simulation. Indenter was positioned on trench center of the 24 nm wide SiNLs.

Friction coefficient μ	Calculated critical buckling load (μN)	Calculated magnitude of displacement burst (nm)
0.02	10	25
0.03	13	36
0.04	17	42

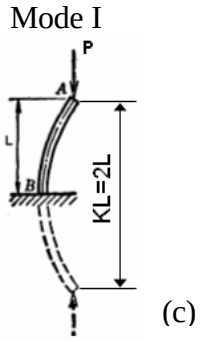
The influence of friction on the magnitude of displacement burst was further interpreted by the simulated indentation curves in Figure 4.7(a). At a displacement of around 45 nm, there is an inflection point (Marked as B in Figure 4.7(a)) indicating an enhancement of stiffness after displacement burst. This was due to the indenter hit the second pairs of SiNLs from the tip, which was described by the circles in the deformation contour of SiNLs in Figure 4.7(b). In Figure 4.7(a), it was shown that as μ increased to 0.05, the predicted displacement burst increased dramatically to ~ 130 nm from A to C. This value was much larger than the magnitude of displacement burst observed in experimental tests.



(a)



(b)



(c)

Figure 4.7 FEM simulation of the SiNLs under indentation. The tip of the indenter was located on top of the trench center. (a) plots of the simulated load-displacement curves. The maximum displacement is 140 nm. Friction coefficient μ changed from 0.01 to 0.05. (b) deformation contour of SiNLs when indentation displacement was at B as marked in (a). The indenter hit the second pairs of SiNLs from the tip, which was indicated by the circles in (b). (c) schematic of buckling mode (Mode I) of SiNLs. The bottom end was fixed and the top end was free.

From the analysis on the critical buckling load and the magnitude of displacement burst, the friction coefficient at the contact was estimated to be around 0.02-0.04 in Deformation Mode I. This value of friction coefficient is larger than that of contact between the indenter with 4.6 μm radius of tip and the 74 nm wide SiNLs, which was about 0.012 (as evaluated in Chapter 3). The discrepancy might be from the difference of contact conditions in these two tests, including different indenters used, different contact

angles, etc. Under this situation the SiNLs buckled outwards to the indenter tip after a critical load. Figure 4.7(c) shows a schematic of the buckling mode, which was named Mode I in this dissertation.

Figure 4.8 shows some simulated indentation curves including both loading and unloading processes. In Figure 4.8(a) under the frictionless condition, the loading and unloading curves followed exactly the same path in the indentation, suggesting no energy dissipation in indentation. With the introduction of friction at the contact, hysteresis of load-displacement curves appeared, indicating work done by the friction force during indentation. However, in Figure 4.8(b) the hysteresis predicted by the simulation was smaller than that in experimental tests. This might be addressed with a more accurate model, *e.g.*, taking into account the dynamic postbuckling behavior, or considering Si substrate in FEM, etc. Applying a close-loop feedback control in the indentation test system may also help to obtain a better indentation control.

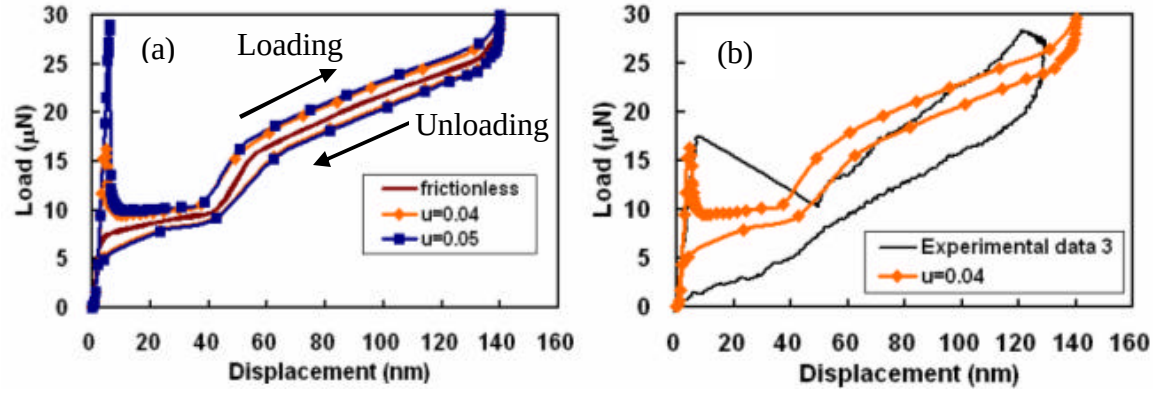


Figure 4.8 FEM simulation of SiNLs under indentation. Both loading and unloading processes were simulated. The indenter was located on top of the trench center. (a) simulated indentation curves. Hysteresis appeared in the load vs. displacement curves with consideration of friction at contact. (b) simulated load-displacement curve and a set of experimental data. Maximum displacement was ~ 140 nm.

To estimate the critical strain to fracture, a finite element simulation was conducted up to 220 nm indentation depth as shown in Figure 4.9. A maximum principal strain of 7.5% was obtained at the bottom ends of the two center lines. Again although the present model might not be accurate for the postbuckling analysis, the bending strain as a geometric measure serves as a reasonable estimation for the deformation of the SiNLs. Since the SiNLs did not fracture up to a 220 nm indentation depth as shown in Figure 4.4(a), the strain to fracture for the SiNLs was estimated to be above 7.5%. Meanwhile, in Figure 4.5(a) for Test i, after buckling in Mode I to a 250 nm displacement, the SiNLs eventually fracture, resulting in a another displacement burst. With a similar FEM simulation and a 250 nm indentation displacement, the maximum principal strain at the bottom ends of the center lines was calculated to be 9.7%, which was an estimation of the upper bound of the strain to failure of the SiNLs.

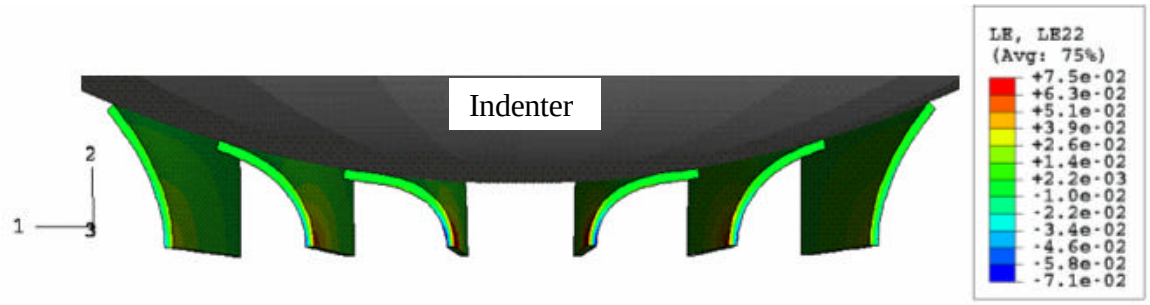


Figure 4.9 FEM simulation shows the deformation of the nanolines with 220 nm indentation displacement indentation on SiNLs. Indenter was located on trench center. As an estimation of the strain to fracture, the maximum principal strain was ~ 7.5%, which was at the bottom end of the two center lines.

4.2.3 Influence of friction on buckling mode of SiNLs

In Figure 4.4(a) it is shown that as the friction coefficient increased from 0.04 to 0.05, the critical load of SiNLs increased significantly form 16 μN to 29 μN. This jump

was found to be directly related to the change of the buckling mode due to the confinement of the top ends of SiNLs by the friction force. In the following part, after a brief description of friction at nano-scale, the effect of friction on buckling mode is discussed.

A Introduction to friction

The well known Amonton–Coulomb friction law is satisfactory for many engineering problems in the real world. The friction force $f = \mu N$, where N is the applied normal load and μ is the so-called friction coefficient. However, this law was obtained from empirical observations. The assumption of this law requires an intimate solid-solid contact. In this case the friction force is proportional to the applied load and independent of the contact area.

In the indentation tests, this assumption may not be strictly fulfilled. As shown in Figure 4.2(b), the indenter surface is relatively rough compared with the linewidth of the SiNLs at nano-scale. In this situation, as the top of SiNLs slides along the rough indenter surface, the contact condition depends on the local geometry of the indenter surface and the SiNLs. The contact area may change during sliding. Consequently, a more general law, based on Bowden and Tabor's assumption, should be used to describe this contact condition. Here the friction force $f = \tau A$, where τ is the shear strength of SiNLs and A is the true contact area. The true contact area may change as the top of SiNLs slide on the indenter surface.

However, in the FEM simulation, for simplicity the Coulomb law was used to characterize the contact friction properties. In this situation, the friction coefficient represents only an "effective" contact property between the indenter and silicon. The change of friction coefficient reflects a change of contact area in the indentation test. In the following discussion, a friction coefficient is still used to describe contact property, but it should be noted that it is influenced by the change of the contact area in the indentation.

B Effect of friction on deformation behavior

In Figure 4.4(a) it is shown that as the friction coefficient increased from 0.04 to 0.05, the critical load of SiNLs increased significantly from 16 μN to 29 μN. To further understand this phenomenon, a FEM simulation was performed with the friction coefficient increased to 0.06 and above. Figure 4.10 shows a deformation contour of the SiNLs with the friction coefficient μ of 0.06 and an indenter displacement of ~ 60 nm. Because the movement of the top ends of the SiNLs was confined by the friction force, the buckling mode of SiNLs changed from bending outwards to bending inwards, corresponding to a pinned boundary condition at the top ends. After buckling, the maximum tensile stresses appeared at both the center and the bottom of the SiNLs, as indicated by the arrows in Figure 4.10(a). Figure 4.10(b) shows a schematic of this buckling mode. For convenience it is named Mode II here.

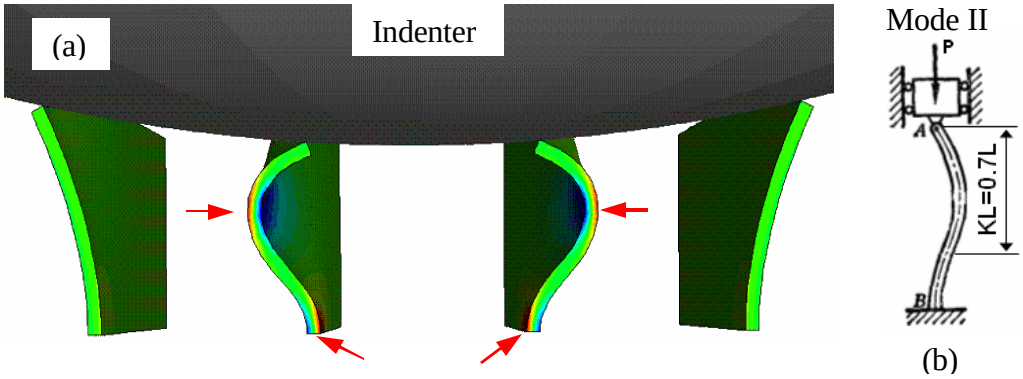


Figure 4.10 (a) FEM simulation shows the deformation contour of the nanolines with friction coefficient μ=0.06. Indenter was located on trench center. Because the movement of the top ends of SiNLs was confined by the friction force, the buckling mode of SiNLs changed from bending outwards to bending inwards, corresponding to a pinned boundary condition at the top ends. After buckling, the maximum tensile stresses appeared at both the central area and the bottom ends of the SiNLs, which was indicated by the red arrows. (b) schematic of buckling mode (Mode II) of SiNLs. The bottom end was fixed and the top end was pinned.

Figure 4.11 shows four sets of simulated load vs. displacement curves with friction coefficient μ ranging from 0.04 to 0.1. When μ was 0.04 or 0.05, Mode I buckling occurred after a critical load. Owing to the change of the buckling mode, as μ increased to beyond 0.06, the simulated indentation curves predicted a higher critical load (~ 55 μN) and a lower magnitude of displacement burst (~ 12 nm in Figure 4.11) than those in buckling Mode I. As friction coefficient μ changed from 0.06 to 0.1, it was shown that the simulated indentation curves agreed with each other well. This indicates that once the friction force increased to a level that traps the movement of SiNLs along the indenter surface, the increase of friction force posed little influence on deformation behavior of SiNLs.

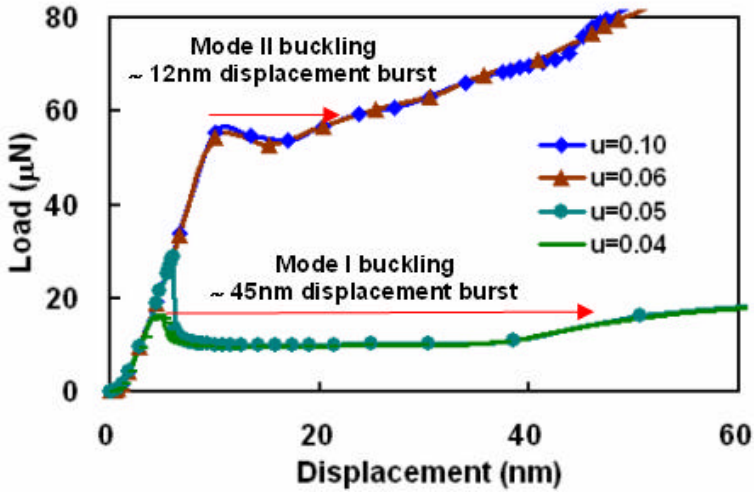


Figure 4.11 Simulated load vs. displacement curves of SiNLs under indentation with Friction coefficient μ changed from 0.04 to 0.10. The indenter was located on top of the trench center. When μ is 0.04 or 0.05, Mode I buckling occurred after a critical load. As μ increased to beyond 0.06, Mode II buckling occurred, predicting a higher critical load and a lower magnitude of displacement burst than those in Mode I buckling.

The function of friction force on the buckling mode of the SiNLs can be further explained by an analysis on the contact geometry between indenter surface and SiNLs, which is shown schematically in Figure 4.12. Here N is the normal force applied by the indenter on the top of SiNLs. The friction force f is along the tangential direction of the indenter surface, and is equal to μN, where μ is the friction coefficient at the contact. Thus, if the total force along x direction is smaller than 0, the SiNLs can slide along the indenter surface:

$$-N*\sin\alpha + f*\cos\alpha < 0 \qquad (4.1)$$

where α is the inclined angle of the indenter surface to the SiNLs. Substitute $f=\mu N$ into Eqs. 4.1, the formula can be reduced to

$$\mu < \tan\alpha \qquad (4.2)$$

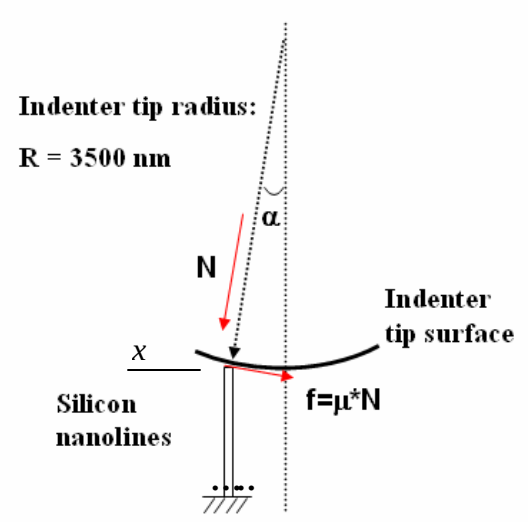


Figure 4.12 Schematic of contact geometry between the indenter surface and the SiNLs. *N* is the normal force applied by the indenter on the top of SiNLs. *f* is the friction force generated between indenter and the SiNLs.

When the inclined angle α is small,

$$\tan\alpha \approx \frac{\text{Half width of the pattern trench}}{\text{Radius of indenter tip}} \tag{4.3}$$

For this set of SiNLs, the pattern trench width was 366 nm. With the tip radius of ~ 3500 nm, tanα is estimated to be ~ 0.05. According to Eqs. 4.2, when μ is smaller than 0.05, the SiNLs could slide along indenter surface, resulting in a buckling behavior of Mode I. Hence 0.05 is a minimum friction coefficient that is required for the SiNLs buckling in Model II.

Figure 4.13 plots the calculated critical load as a function of the friction coefficient μ used in FEM modeling, with μ varying from 0 to 0.1. The FEM results are in good agreement with the prediction of Eqs. 4.2, showing a buckling mode transfer at a critical friction coefficient of 0.05. For deformation behavior 1, the friction coefficient

was estimated to be around 0.02-0.04, and the SiNLs buckled in Mode I in the indentation.

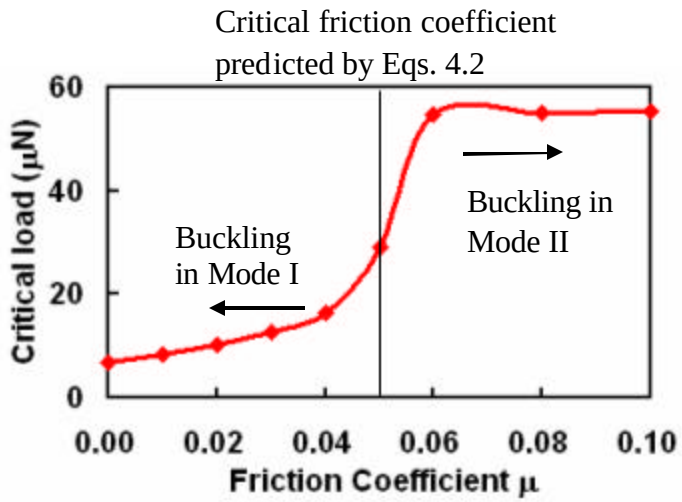


Figure 4.13 The critical indentation load predicted by the finite element model, as a function of the friction coefficient between the indenter tip and the 24 nm Si nanolines.

It is shown in Figure 4.13 that as the friction coefficient μ ranged from 0.04 to 0.06, the calculated critical load was very sensitive to the change of friction properties. Thus a friction coefficient μ of 0.04-0.06 is like a transition zone inducing transferring between the two buckling modes. Since in the real test due to the possible dynamic effect of loading, plus the contact between the indenter and the SiNLs is not as homogenous as that assumed in simulation, the top ends of SiNLs in this transition zone may or may not slide along indenter surface. This might be the reason leading to Deformation Mode II as shown in Figure 4.4(b).

Figure 4.14 shows plots of the simulated load-displacement curves with friction coefficient μ equals to 0.05 and 0.06, respectively, and the indentation experimental data of Deformation Mode II (curves in Figure 4.4(b)). It was shown that the FEM results

matched reasonablely well the experimental data in the elastic part. The critical loads of the three tests were in a range of 24 μN to 30 μN, corresponding to a friction coefficient of 0.05. However, the magnitude of displacement burst was much smaller than that predicted by FEM simulation as shown in Figure 4.14. One possible explanation is that after displacement burst, the top ends of the SiNLs slided along the indenter surface for some distance, and then were retrapped by the friction force. The buckling behavior was mainly a Mode II behavior with some elements of Mode I, which is shown in the schematic in Figure 4.14(b). The buckling behavior is named Mode II.a for convenience. In this case the maximum tensile stresses appeared at both the central area and the bottom ends of the SiNLs, which was shown in Figure 4.10(a). This also explained the mud-like pieces in the indent of Deformation Mode II as indicated in Figure 4.5(c).

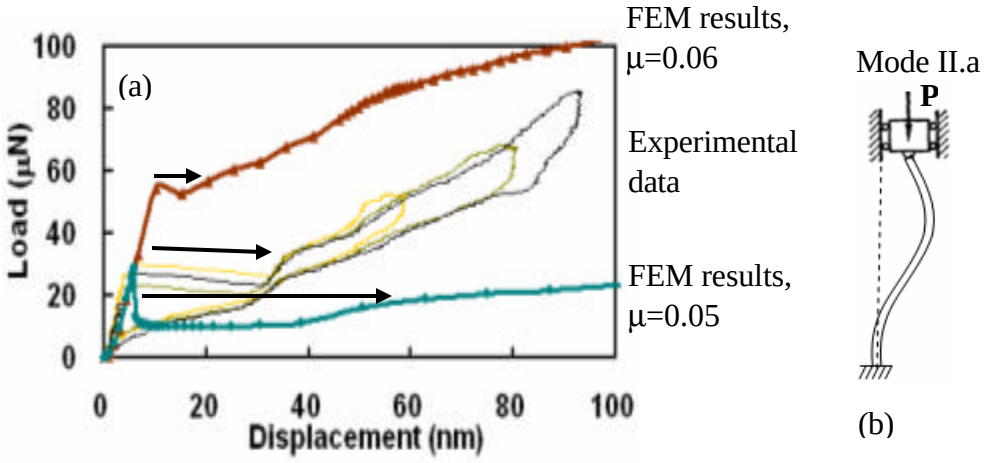


Figure 4.14 plots of the simulated load-displacement curves with friction coefficient μ=0.05 and 0.06, and the indentation experimental data of Deformation Mode II (curves in Figure 4.4(b)). The magnitude of displacement burst in each case was indicated by arrows. (b) schematic of buckling mode (Mode II.a) of SiNLs. The bottom end was fixed, the top end slides and then was pinned.

4.2.4 Summary of analysis on indentation results of 24 nm wide SiNLs

In summary, a finite element model was used for simulation of the initial elastic response, prediction of the critical load, and determination of the magnitude of displacement burst. The elastic modulus of the 24 nm SiNLs was found to be similar to its bulk, showing an insensitivity to the scaling effect. The strain to fracture of the 24 nm SiNLs was estimated to be between 7.5% and 9.7%, which is comparable to that of the 74 nm wide SiNLs (~8.5%) as estimated in Chapter 3. The friction coefficient at the contact between the indenter and the SiNLs was determined to between 0.02 to 0.05. Under indentation, SiNLs buckled in Mode I or Mode II.a behavior, depending on the friction properties at the contact. In the following analysis, a similar approach was employed to extract materials properties of the 90 nm wide SiNLs.

4.3 Nanoindentation on 90 nm wide SiNLs

Figure 4.15 shows plan-view and cross-sectional SEM images of the SiNL set 2. The line width and the height of these SiNLs were about 90 nm and 1400 nm, corresponding to a AR of 15. The line pitch was 450 nm and the trench width of the pattern was 360 nm, which was close to that of the SiNL set 1 (~ 183 nm) and had a similar $\tan\alpha$ of 0.05, where α is the inclined angle between the indenter and the SiNLs.

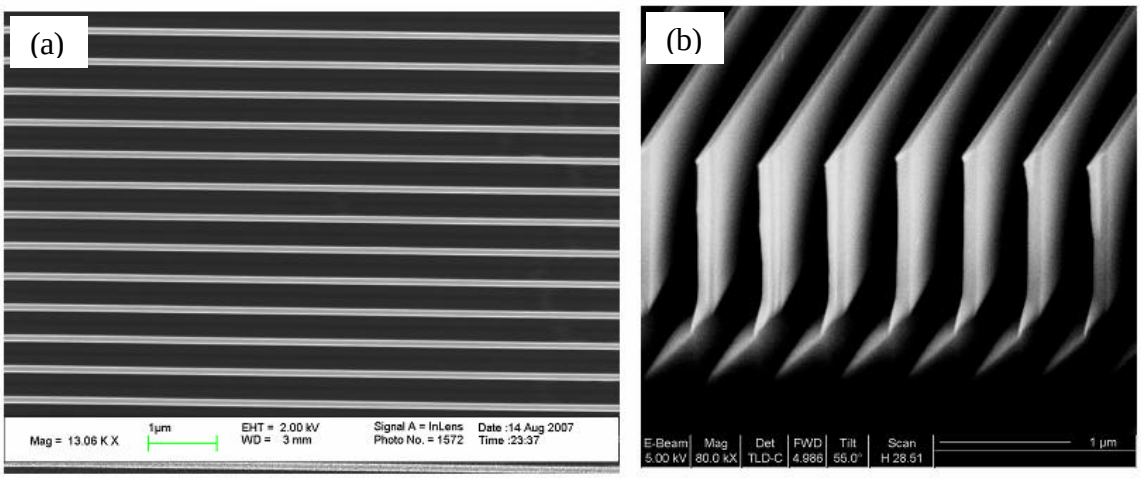


Figure 4.15 SEM images of the parallel silicon nanolines, with 90 nm line width and 1400 nm height. The line pitch is 450 nm. (a) Plane view; (b) Cross-sectional view with 60° tilt angle. A small trench pattern is specially designed at one end of the line to facilitate the cross-sectional SEM imaging, showing the sharp edges due to the anisotropic etching.

4.3.1 Analysis of the buckling behavior during indentation

Figure 4.16(a) shows 13 force-displacement curves obtained from nano-indentation tests of the 90 nm wide SiNLs. The displacement was fully recovered and no residual deformation was observed after withdrawal of the indenter. Compared with the indentation response of the 24 nm wide SiNLs, the critical buckling load increased dramatically to a range between 100 μN to 200 μN. This increase was mainly attributed to the change of linewidth, since both of the SiNLs had a similar AR. The distribution of critical load followed normal distribution function. Figure 4.17 plots the cumulative probability function (CDF) of the critical buckling load in Figure 4.16(a). The CDF curve was fitted by the addition of two normal distributions of critical load. One of the critical

load distributions had a mean value of 117 μN and a standard deviation of 12 μN. For another normal distribution, the mean was 198 μN and the standard deviation was 1 μN.

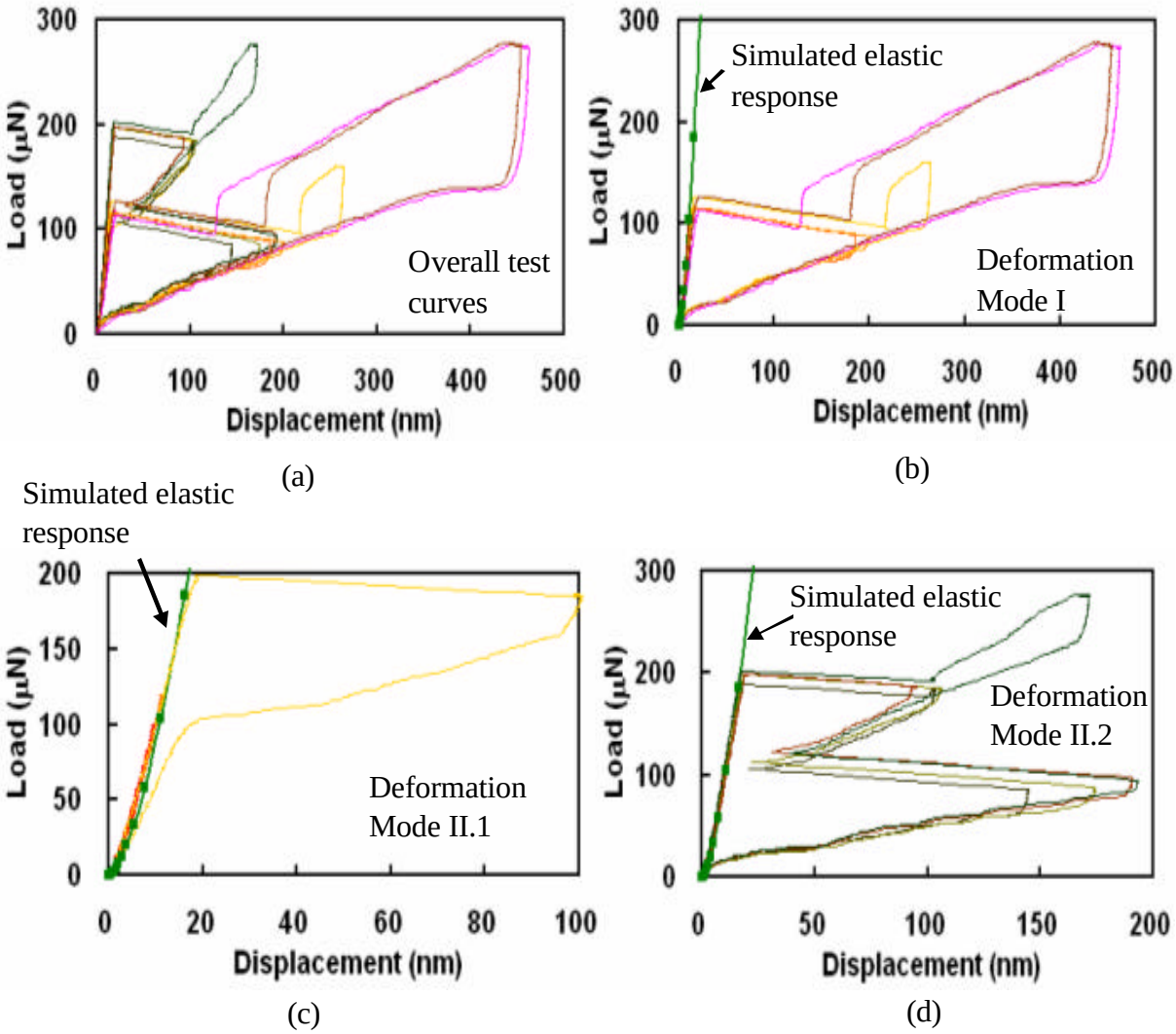


Figure 4.16 Load vs. displacement curves of nanoindentation tests of the 90 nm wide SiNLs with 1400 nm height. Indenter was located on the pattern trench center. (a) For these 14 indentation tests, no residual deformation was observed after withdrawal of the indenter. Different deformation modes were observed: (b) Deformation Mode I: Critical load was ~120 μN. (c) Deformation Mode II.1: critical load is ~ 200 μN. (d) Deformation Mode II.2: critical load is ~ 200 μN. And the indentation curves have a second displacement burst occurred during the unloading process. For Deformation Mode II.1 and II.2, they have similar critical load and magnitude of the first displacement burst.

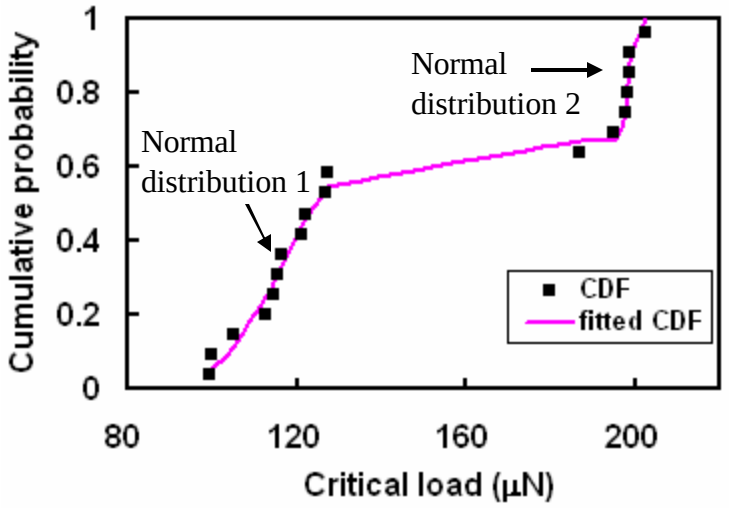


Figure 4.17 Cumulative probability function (CDF) plot of the critical buckling load of indentation of the 90 nm wide SiNLs. The CDF curve was fitted by the addition of two normal distributions of critical load. Normal distribution 1: Mean = 117 μN, standard deviation = 12 μN; Normal distribution 2: Mean = 198 μN, standard deviation = 1 μN;

According to the critical load level, the deformation behavior can be divided into two major modes. In Deformation Mode I as shown in Figure 4.16(b), the critical load was around 117 μN. The maximum indentation displacement was ~ 450 nm, which was about 1/3 of the line height. For Deformation Mode II in Figure 4.16(c) and Figure 4.16(d), the critical load was ~ 200 μN, and the maximum indentation displacement was below 200 nm. Interestingly, it was observed that in some of indentation curves of Deformation Mode II, a second displacement burst occurred during the unloading process as indicated in Figure 4.16(d). These indentation behaviors will be explained in the following part.

The indentation results were analyzed using FEM simulation. Similar to the FEM analysis of nanoindentation of 24 nm wide lines, the simulated indentation curves are in

agreement with those of experimental data in the elastic part, which was shown in Figure 4.16 (b), (c) and (d). Figure 4.18 shows the calculated critical load as a function of the friction coefficient μ by FEM modeling, with friction coefficient ranging from 0 to 0.1. Since this set of SiNLs also had a $\tan\alpha$ of 0.05, the FEM results showed a buckling mode transfer at a critical friction coefficient of 0.05, which is similar to the plot in Figure 4.13. It is noted that in Figure 4.18 the critical load transition zone for transfer of buckling modes ranged from 0.04 to 0.07. This range was larger than that of 24 nm wide SiNLs, which is 0.04-0.06 in Figure 4.13. This may due to the effect of the recovery force from wider SiNLs. To trap the movement of the top ends of SiNLs, the friction force need to exceed the force exerted by SiNLs tending to bounce back to release their deformation. (See Figure 4.10). Thus in Figure 4.18, a higher friction coefficient (~0.07) was required to fully confine the movement of the top ends of SiNLs for buckling of SiNLs in Mode II to occur.

For Deformation Mode I of indentation on 90 nm wide SiNLs (See Figure 4.16(b), with a critical load ~117 μN), the friction coefficient between the indenter surface and the SiNLs was estimated to be around 0.04 (the calculated critical load was 112 μN from Figure 4.18). In this case the SiNLs buckled in Mode I (bending outwards to indenter) during the indentation. For Deformation Mode II (including the Mode II.1 in Figure 4.16(c) and II.2 in Figure 4.16(d)), with the critical load of ~ 200 μN, the friction coefficient was estimated to be ~ 0.05 as indicated in Figure 4.18. According to the previous analysis on the Deformation Mode II of indentation of the 24 nm wide SiNLs (See Figure 4.14), Mode II.a buckling occurred in the indentation, which corresponded to

the displacement burst in Figure 4.16(c) and the first of the two displacement bursts in Figure 4.16(d).

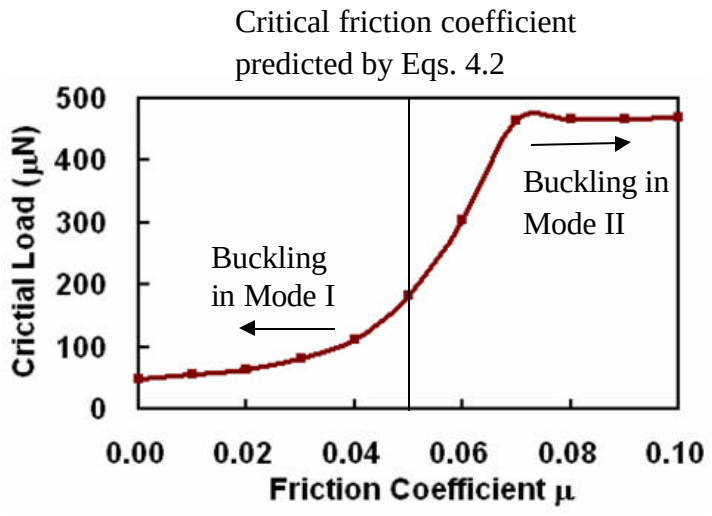


Figure 4.18 The critical indentation load predicted by the finite element model, as a function of the friction coefficient between the indenter tip and the 90 nm Si nanolines.

In the indentation curves of Figure 4.16(d), a second displacement burst was observed during the unloading process. To facilitate better understanding of the indentation experiments, particularly the tests in Figure 4.16(d), it should be noted that indentation was load-controlled, instead of being displacement-controlled. It was noted that the indentation curves of the second displacement burst, including the critical load, the magnitude of displacement burst, and the slope of the unloading curve after the burst, matched well with those of the displacement burst in Figure 4.16(b). This indicated that the second displacement burst followed the same buckling mode of the Deformation Mode I. Thus the behavior suggested an occurrence of a buckling mode transfer during unloading from buckling Mode II.a to buckling Mode I during the displacement burst.

The initiation of the buckling mode transfer was attributed to the influence of friction in indentation. Figure 4.19 shows a schematic of the effect of friction on buckling mode transfer. In generally, the friction force *f* is on the tangential direction along indenter surface. In loading, *f* tends to suppress the occurrence of buckling mode transfer, which is shown in the Figure 4.19(a). However, in unloading since the withdrawn of the indenter is the trigger of unloading, which seems before the SiNLs can respond, the friction force changes sign in this case. This may lead to the shape of nanoline transforming from bending inwards (Mode II.a in Figure 4.19(b)) to bending outwards (Mode I), leading to soften of the nanoline structure. In a load-controlled experiment, this predicts a displacement burst in unloading.

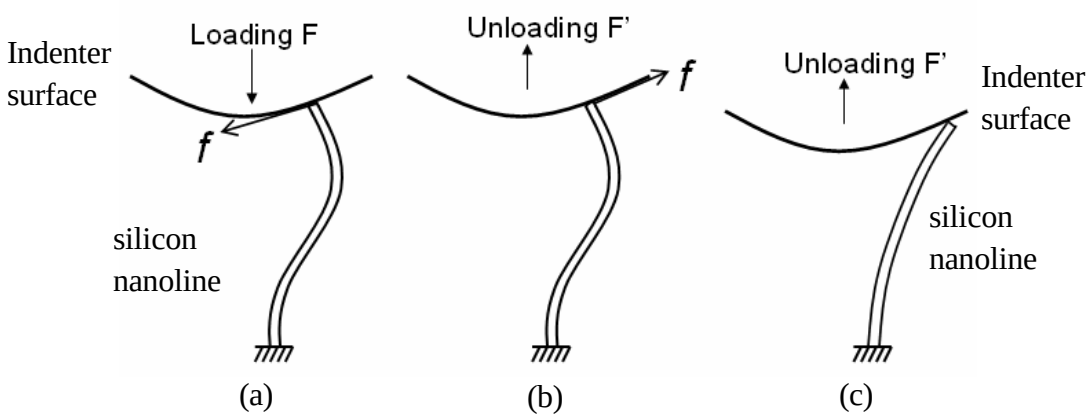


Figure 4.19 Schematic of the effect of friction on buckling mode transfer. *f* is the friction force generated at the contact between indenter surface and the silicon nanoline. (a) In loading process, friction force tended to suppress nanoline from buckling. (b) in unloading, friction force changed sign, facilitating a buckling mode transfer from Mode II.A to Mode I, which is indicated in (c).

It is noted that for indentation of the 24 nm wide SiNLs, in a similar Deformation Mode II, the mode transfer in unloading did not occur. This may be due to a higher

recovery force for wider nanolines bouncing back to its original shape, which facilitates the occurrence of this mode transfer.

4.3.2 Analysis of fracture of SiNLs

To estimate the critical strain to fracture, finite element simulation was conducted up to 450 nm indentation depth as shown in Figure 4.20. A maximum principal strain of 3.8% was obtained at the bottom ends of the two center lines. Since the SiNLs did not fracture up to a 450 nm indentation depth as shown in Figure 4.16(b), the strain to fracture for the SiNLs was estimated to be above 3.8%.

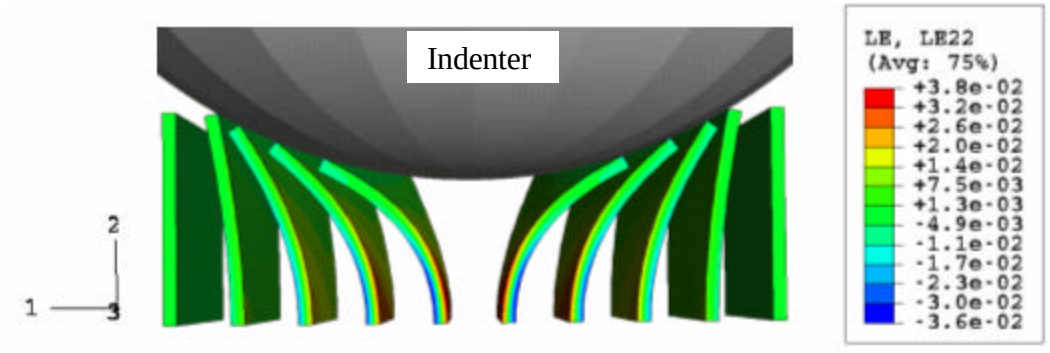
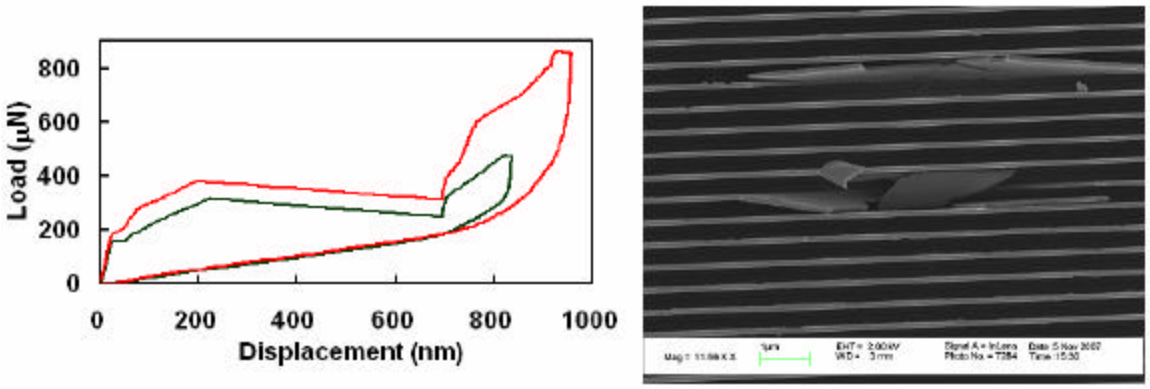


Figure 4.20 FEM simulation shows the deformation of the nanolines with 450 nm indentation displacement indentation on SiNLs. Indenter was located on trench center. As an estimation of the strain to fracture, the maximum principal strain was ~ 3.8%, which was at the bottom end of the two center lines.

Fracture of SiNLs can occur with higher indentation loading and was observed. Figure 4.21(a) shows two indentation curves with residual deformation left after unloading. The critical loads of these two tests are close to 180 μN, corresponding to Mode II. A buckling after the first displacement burst. Figure 4.21(b) shows a SEM image of the fractured SiNLs after these two indentation tests. It was found that in both indents,

only one nanoline fractured even with indenter locating on trench center of the SiNLs. This may be attributed to a deviation of symmetric indentation condition, for example, when the indenter deviated slightly from the trench center, or a change of the localized contact geometry between the two nanolines and indenter, etc. The nanoline was broken into pieces, which may due to buckling in Mode II.A.



(a) (b)

Figure 4.21 Fracture of the SiNLs led to large residual displacement after unloading of the indenter. (a) Load vs. displacement curves of two indentation tests. (b) SEM image of the fractured SiNLs.

Since only one nanoline fractured after indentation, this indicates that after a maximum displacement of ~950 nm as shown in Figure 4.21(a), one of the two center nanolines still survived after indentation. With a FEM model similar to Figure 4.20 and a maximum displacement of 950 nm, the upper bound of the 90 nm SiNLs was estimated to be ~9.1%.

4.4 Summary of nanoindentation analysis

In summary, nanoindentation technique together with FEM simulation was used to characterize mechanical properties of two sets of SiNLs, having an AR of 16 and feature size scaled down to 24 nm. The elastic modulus of the SiNLs was found to be similar to its bulk, showing an insensitivity of modulus to the scaling effect. Buckling instability was analyzed by FEM simulation, based on the predicted critical load, magnitude of displacement burst, etc. Deformation behaviors in the indentation tests were investigated, showing that the buckling response of the SiNLs was a combined effect of load, line geometry, and the friction properties at the contact.

Mechanical properties of the SiNLs, including elastic modulus, strain to failure, and friction properties were extracted from the analysis of the indentation results. Table 4.3 summarizes of the results. Friction properties at nanoscale were characterized, and the friction coefficient was found ranging from 0.01 to 0.05. These values were much smaller than the friction coefficient in macro scale (> 0.1). This interesting result may be due to localized contact area at nanoscale and should be further investigated. At the nanoscale dimension, friction coefficient is influenced by contact area variations. Meanwhile, the friction property at the contact was found to play an important role in controlling buckling mode of SiNLs.

The strain to fracture of the three set of SiNLs was estimated ranging from 3.8%-9.7%, based on the evaluation of the maximum strain at the bottom ends of SiNLs under the maximum magnitude of bending. One conclusion was that the strain to failure of Si at nanoscale was much higher than its bulk (~1%), showing a scaling effect of silicon

fracture strength from the bulk to nano-dimension. However, from these three tests, the results are too limited for qualifying the scaling effect of silicon strength from 24 nm to 90 nm, since there was a distribution of the measured fracture strength of the SiNLs. More experimental data may be needed for the statistical analysis to further understand the dimension dependence of fracture strength. Or a surface polishing process might be useful, by slightly oxidizing surface of SiNLs and then use HF to etch off the formed oxide, to reduce the surface defects as well as the measured data scattering. Another concern was about the validity of the rigid substrate assumption for the extraction of strain to failure. More sophisticated model is required to improve the simulation.

Table 4.3 Summarized indentation tests of the three sets of SiNLs.

		SiNL set 0	SiNL set 1	SiNL set 2
Line Dimension (nm)	Width	74	24	90
	Height (AR)	510 (6.9)	380 (15.8)	1400 (15.6)
	Pitch (Trench width)	180 (106)	390 (366)	450 (360)
Critical Buckling Load (μN)		480-700	9-30	100-200
* Maximum displacement and its ratio to line height (nm)		90 (17%)	220 (58%)	450 (32%)
*Friction coefficient		~0.01	0.02-0.05	0.04-0.05
Strain to failure		~8.5%	7.5%-9.7%	3.8%-9.1%

* Maximum displacement: the maximum displacement in indentation tests, without residual deformation after withdraw of indenter.

* Friction coefficient: for nanoscale contact, here it is an indicator of the contact area variation between the SiNLs and the indenter surface.

Note: Elastic modulus of the SiNLs was similar to silicon bulk. No scaling effect found.

So far no experimental data have been reported on mechanical characterization of Si nano-structures with feature size smaller than 70 nm. As mentioned before, challenges abound from specimen preparation, transducer resolution and interpretation of measurement data at the nano-scale. In this study, feature size as small as 24 nm SiNLs were characterized with a good repeatability of data together with finite element simulation. This study demonstrated a valuable approach for characterization of mechanical properties at the nanoscale.

Chapter 5 Phase Formation and Electron Transport in Nickel Silicide Nano-lines

The first part of this chapter discusses the phase formation of nickel silicide under different conditions. The control parameters presented include annealing temperature, as-deposited nickel thickness, the reacted Ni-Si ratio and linewidth of nano-structures. Phase information and the silicide profile were investigated by using high-resolution transmission electron microscope (HRTEM) to perform micro-structural analysis with feature size down to 15 nm. The second part of this chapter focuses on characterization of the electrical properties of silicide nanolines. For this purpose, a four probe electrical test structure for silicide measurement was designed and fabricated in the device layer of a (110) SOI wafer. The electrical test results showed that the residual resistivity of the silicide lines at cryogenic temperature increased with decreasing line width, indicating an increased electron sidewall scattering with decreasing line width.

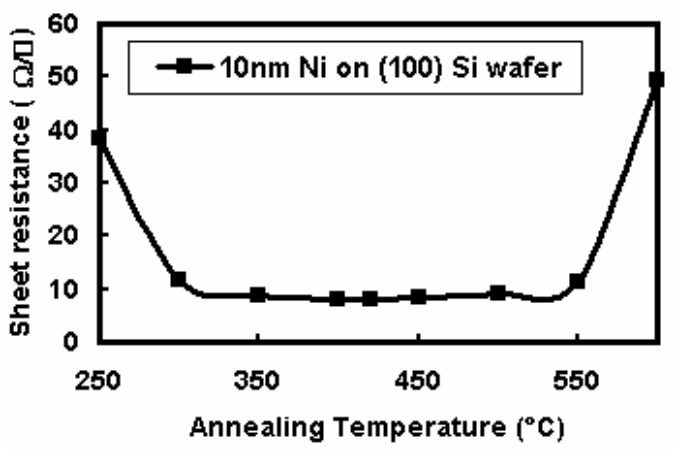
5.1 Nickel Silicide Solid State Reactions and Micro-structural Analysis

Nickel silicide is a metal-silicon compound formed by reacting nickel (Ni) and silicon at an annealing temperature range of 250 ºC to 700 ºC [75,116,117]. It is reported that the formation of low resistivity nickel mono-silicide (NiSi) features was related to not only the annealing temperature, but also to the linewidth in Ni fully silicided (FUSI) gate formation [17,118]. For further investigation on nickel silicide formation at a smaller scale, some control parameters and the corresponding effects in the annealing process were studied. Firstly the influence of the annealing temperature on Ni silicide formation

is presented. It is followed by a study of silicide formation with various thicknesses of the as-deposited Ni coating. Then the influence of the reacted Ni-Si ratio is investigated by the formation of silicide on SOI wafers. These three studies were based on the analysis of nickel silicide films formed on silicon wafers. As for the linewidth effect study, it was conducted on nickel SiNLs with a feature size down to 15 nm, which was formed by annealing a nickel layer coated on the silicon nanolines. Finally, a summary of nickel silicide formation is presented.

5.1.1 Influence of annealing temperature on silicide formation

In the annealing process, the formation of nickel silicide, by Ni diffusing into Si, involves multiple number of phases. However, it is well known that the predominant phases are Ni-rich silicide, NiSi, and $NiSi_2$. Among these, nickel mono-silicide (NiSi) has the lowest resistivity and there is an correlation between the thickness of each layer: 1 nm Ni + 1.8 nm Si → 2.2 nm NiSi [73,116]. In a preliminary exploration of the formation conditions, ~ 10 nm Ni was coated on a (100) silicon wafer by e-beam evaporation and then annealed at temperatures ranging from 300 °C to 700 °C for 1 minute. The un-reacted Ni was removed by a wet etchant (H_2O_2 : H_2SO_4 : H_2O=1:1:4). Figure 5.1(a) shows the measured sheet resistance as a function of annealing temperature after removal of un-reacted nickel by the selective etching process.



(a)

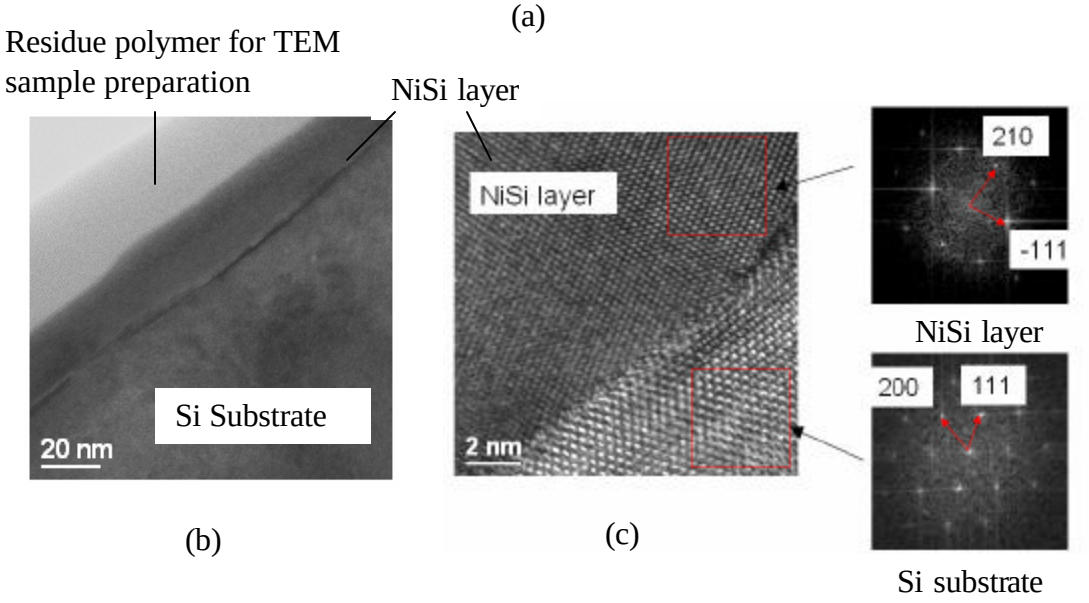


Figure 5.1 (a) The measured sheet resistance of nickel silicide films as a function of annealing temperature. The thickness of the as-deposited Ni is ~ 10 nm. The lowest sheet resistance corresponds to formation of nickel monosilicide. (b) Cross-sectional TEM images of sample after NiSi formation at 420°C. A nickel silicide layer was formed on top of the silicon substrate after annealing. (c) HRTEM image around the interface area. The silicide layer is identified to be orthorhombic nickel monosilicide, with $[1\bar{2}3]$ zone axis parallel to Si $[0\bar{1}1]$ zone axis, which is determined by the two dimensional Fourier transform of images of the selected areas in the silicide region and silicon substrate, respectively.

At low temperatures, the Ni-rich phase formed at around 300°C. As the annealing temperature increased, nickel diffused into the adjacent silicon rapidly and formed low

resistivity nickel mono-silicide. With the annealing temperature higher than 550°C, nickel di-silicide, with its undesirably higher resistivity, formed. It was noticed that, above 300°C, the deposited nickel film was completely consumed during the annealing process. This behavior was substantiated since there was no difference of sheet resistance before and after the removal of un-reacted nickel by the selective etching process. Figure 5.1(b) shows a cross-sectional TEM image of a sample after annealing at 420°C for 1 minute, in which the formation of a ~ 22 nm crystalline silicide layer on top of the (100) crystalline silicon substrate is revealed. From the HRTEM image in Figure 5.1(c), the silicide layer was identified to be the orthorhombic nickel mono-silicide, (space group pnma, a=0.523 nm, b=0.326 nm, c=0.566 nm) with its $[1\bar{2}3]$ lattice vector parallel to $[0\bar{1}1]$ zone axis of silicon. According to the "bath-tub"-like sheet resistance profile, it is shown that, when annealed in a temperature ranging from 350°C to 420 °C, nickel mono-silicide (NiSi) formed from the reaction between the 10 nm Ni layer and the underneath Si. The average sheet resistance of the NiSi film was measured to be ~ 8.3 Ω/ , which corresponded to a resistivity of around 18.3 μΩ·cm. This is in good agreement with published value of 12-20 μΩ·cm [76,119].

5.1.2 Influence of as-deposited Ni thickness on silicide formation

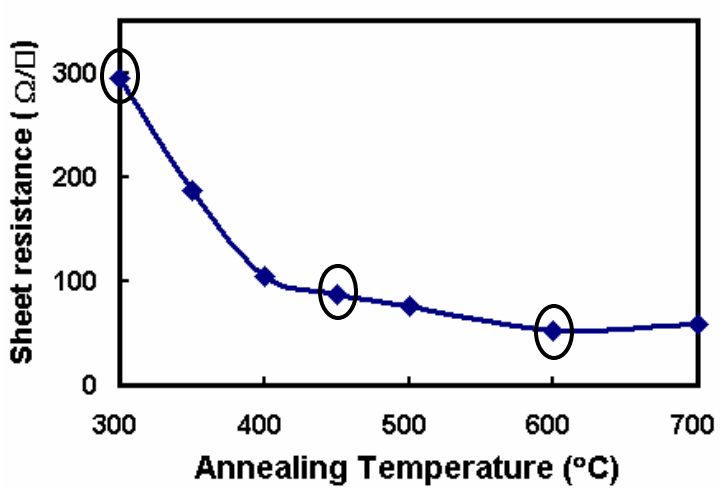
In this study, a ~ 2.5 nm Ni layer was coated on some (100) silicon wafers by e-beam evaporation, and then annealed at temperatures ranging from 300 °C to 600°C for 1 minute. The purpose of the experiment was to form a very thin NiSi layer, and to

investigate its conductivity change due to surface scattering effect in electron transport. Figure 5.2(a) shows the measured sheet resistance as a function of annealing temperature. Interestingly, it was found that the profile of curve was not "bath-tub"-like. The sheet resistance increased almost one order of magnitude higher than that in Figure 5.1(a), although the thickness of the as-deposited Ni was only 1/4 of that of Ni layer in Figure 5.1. Figure 5.2(b), (c) and (d) show cross-sectional HRTEM images of samples annealed at 300°C, 450°C and 600°C, respectively. The images show a silicide layer was formed on top of the silicon substrate after annealing. At the annealing temperature as low as 300°C, the silicide was ~ 5 nm thick, showing an amorphous state as indicated in Figure 5.2(b). The resistivity was determined to be as high as ~ 147 μΩ×cm. As the annealing temperature increased, the measured sheet resistance kept decreasing. Figure 5.2(c) shows a HRTEM image of a sample annealed at 450°C. It is noted that a coherent interface formed between silicide layer and the Si substrate underneath. The silicide layer was determined to be cubic Ni disilicide ($NiSi_2$, space group $Fd\bar{3}m$, lattice constant a=0.5416 nm), whose lattice constant was almost identical to that of Si (a=0.5431 nm). The thickness of the $NiSi_2$ layer was ~ 8 nm, and the resistivity is estimated to be ~ 70 μΩ×cm. It is also noted there were some pyramidal grains grown into the Si substrate. In Figure 5.2(d), it is shown that as the temperature increased to 600°C, these pyramidal grains disappeared and the resistivity reduced to 43 μΩ×cm, which is about 1.5 times as higher as that of NiSi layer formed with 10 nm thick as-deposited Ni.

This expitaxy between $NiSi_2$ and Si interface is due to the excellent lattice match between them. Figure 5.3 shows a HRTEM image of the area around the pyramidal grain

in Figure 5.2(c) and the corresponding two dimensional Fast Fourier Transformation (FFT) image. The image showed an excellent interface match and faceting of grain along {111} planes. This was due to the low interface energy along the {111} plane, providing a driving force for {111} faceting [73,120]. These facets do not appear to be energetically stable. For example, as annealing temperature increased to 600°C, they disappeared resulting in a smoother interface as shown in Figure 5.2(d) as well as a lower sheet resistance plateau shown in Figure 5.2(a).

It is well known that NiSi formation temperature window is from 300°C to 550°C. However this study shows that, for ultra-thin as-deposited Ni, the phase vs. temperature profile was quite different from that of a thicker Ni coating. At 450°C, $NiSi_2$ instead of NiSi was formed on top of the Si substrate, and showed a much smoother coherent interface. Based on these observations, it is assumed that in the annealing process, Ni diffused into Si, initially forming Ni-rich amorphous silicide as shown in Figure 5.2(b). This layer was unstable with respect to crystallization. As annealing temperature increased, crystalline NiSi nucleated and grew, and the concentration shifted to 1:1, which is shown in Figure 5.1(b). However, for ultra-thin Ni coating as thin as 2.5 nm, diffusion of Ni into Si could be fast enough to overcome the thermodynamic barrier, forming a more stable $NiSi_2$ phase and a coherent interface at a relative low annealing temperature, which is shown in Figure 5.2(c) and (d).



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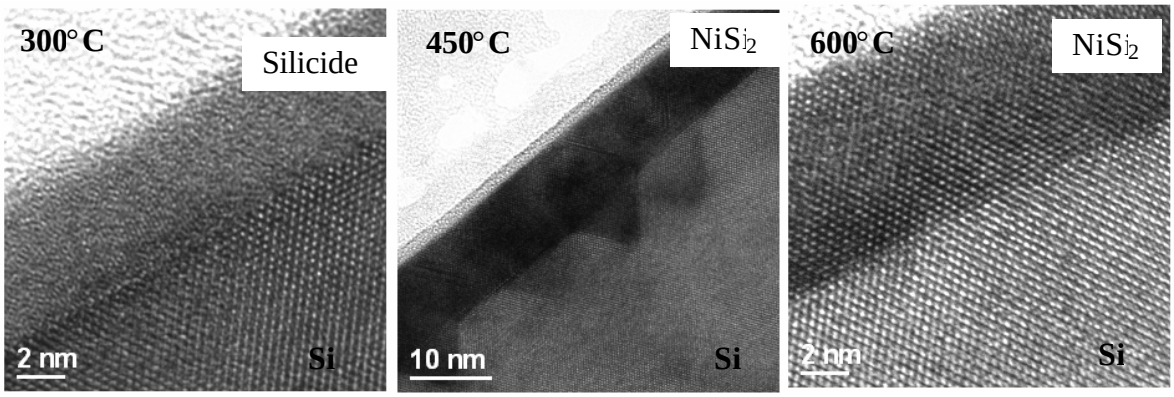
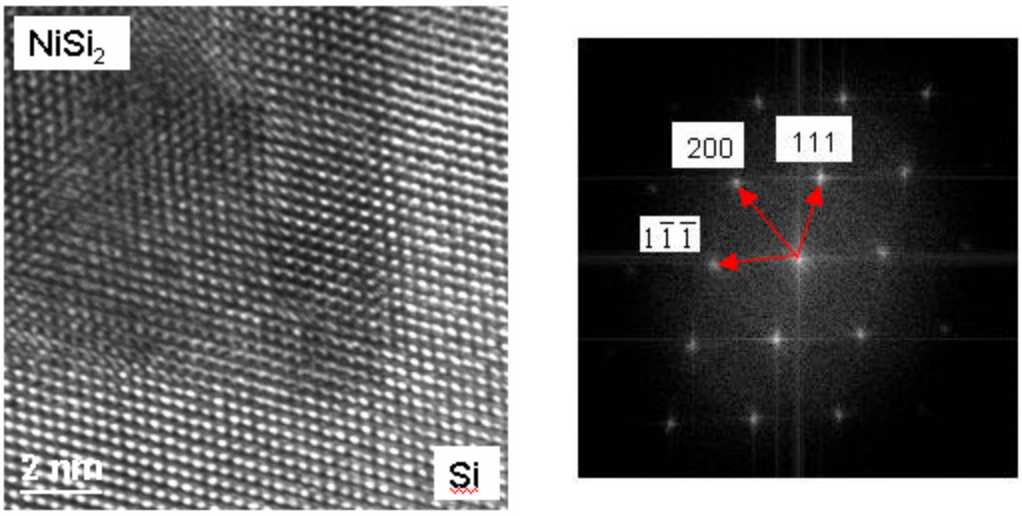


(b) (c) (d)

Figure 5.2 (a) The measured sheet resistance of nickel silicide films as a function of annealing temperature. The thickness of as-deposited Ni is ~ 2.5 nm. (b), (c) and (d) are cross-sectional HRTEM images of samples annealed at 300°C, 450°C and 600°C, respectively. A nickel silicide layer was formed on top of the silicon line after annealing. (b) Silicide was ~ 5nm thick, showing an amorphous state. The resistivity was ~ 147 μΩ×cm. In (c) and (d): a ~8 nm thick $NiSi_2$ layer formed coherently into Si substrate. In (c) there were some pyramidal grains grown into Si. Resistivity was ~ 70 μΩ×cm. As annealing temperature increased to 600°C, pyramidal grains disappeared and the resistivity reduced to 43 μΩ×cm.



(a) (b)

Figure 5.3 (a) A HRTEM image of the area near the pyramidal grain. (b) Two dimensional fast Fourier transformation (FFT) image of (a). The images showed an excellent interface match and faceting of grain along {111} planes.

In an extreme case, if only one lattice layer of Ni was coated on Si, it could react with Si atoms at an even lower temperature to form an expitaxal silicide layer. This process is called template process, which was previously used to form single crystalline NiSi in an ultra-high vacuum (UHV) system [121].

5.1.3 Influence of the reacted Ni-Si ratio on silicide formation

To study the electron transport in nickel silicide, SOI wafers were patterned as electrical test structures. In the nickel silicide formation on SOI wafer, it was observed that the sheet resistance of silicide layer was not only dependent on the annealing temperature, but also related to the reacted Ni-Si ratio, which is defined as the volume ratio of Ni to Si available in the silicide formation. The phenomenon was observed from

the NiSi formation tests where a ~ 90 nm thick Ni layer was evaporated on both bulk (110) silicon wafers and on a (110) SOI wafer. For this set of SOI wafers, the thicknesses of the Si device layer and the buried oxide layer were 60 nm and 150 nm, respectively. The annealing temperature was 550°C and the dwell time was 1 minute. For silicide formation on the (110) bulk silicon, the sheet resistance was measured to be 0.7 Ω/ , indicating that a ~ 200 nm thick NiSi layer had formed with a resistivity of ~ 14 μΩ×cm. (There were no differences of sheet resistance before and after the removal of un-reacted nickel by the selective etching process, indicating all the Ni layer was consumed after annealing.) However, for silicide formation on the (110) SOI wafer, the sheet resistance was unexpectedly as high as 5.9 Ω/ , which was almost one order of magnitude higher than that on the (100) wafer. Assuming that the entire Si device layer of the SOI wafer was consumed to form NiSi, which would have needed only a 33 nm thick Ni to complete the reaction, the thickness of NiSi layer should be ~ 73 nm, leading to a ~ 43 μΩ×cm resistivity. This value was almost twice the resistivity of NiSi, indicating that although the annealing was in the temperature window of formation of NiSi, other silicide phase might form and contribute to this unexpected high resistivity.

HRTEM was then performed to analyze the microstructure of the silicide layer. Figure 5.4(a) shows a cross sectional TEM image of silicide layer on top of the SOI wafer. It was found that the thickness of the polycrystalline silicide layer was ~ 100 nm instead of ~ 73 nm. Figure 5.4(b) shows a HRTEM image including crystalline lattice fringes inside one silicide grain. From the two dimensional FFT image of Figure 5.4(b), the phase was determined to be high resistivity δ-Ni_2Si (Orthorhombic, space group

Pbnm, a=7.06Å, b=4.99Å, c=3.72Å) instead of NiSi. This also explains the formation of a ~ 100 nm thick silicide layer, because for Ni_2Si formation, the interrelation among the thickness of each layer is 1 nm Ni + 0.9 nm Si → 1.5 nm Ni_2Si [116].

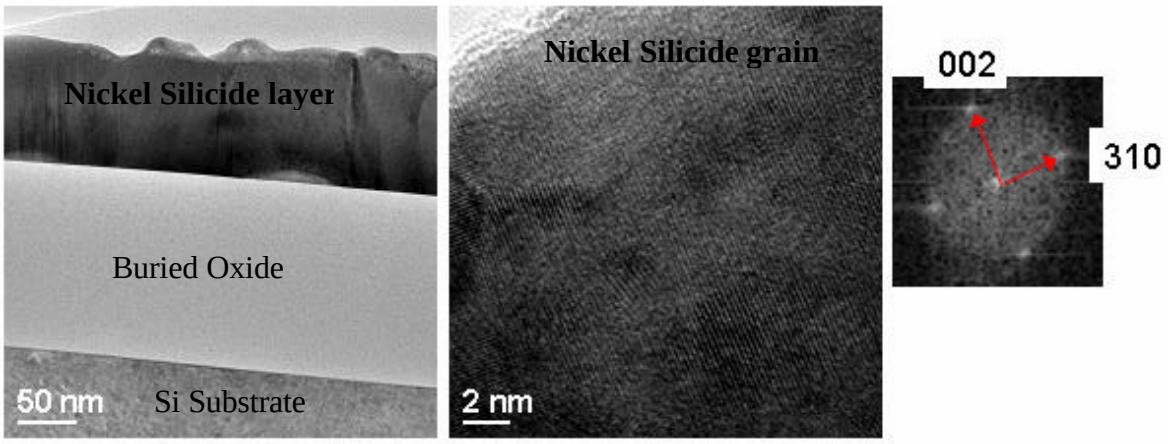


Figure 5.4 (a) Cross sectional TEM image of silicide formation on SOI wafer. The thickness of the polycrystalline silicide layer was ~ 100 nm. (b) HRTEM image of the area inside one silicide grain, showing crystalline lattice fringes. From the two dimensional FFT image of (b), the phase was determined to be δ-Ni_2Si.

This phenomenon could be explained by the Ni-Si reaction path. If the Si source is unlimited and Ni is coated on Si substrate, after the formation of Ni-rich silicide, NiSi will be formed where Ni diffused into adjacent Si. Here, 1 nm of Si needs to react with 0.56 nm Ni to form 1.2 nm NiSi. But, if there exists extra Ni, and Si is fully consumed after the initial growth of the Ni-rich silicides, NiSi cannot nucleate even at the proper annealing temperature. In this case, with the presence of excessive Ni, Ni_2Si was formed even at an annealing temperature as high as 550°C. This observation is very similar to that reported in reference [17], showing that when annealed at 520°C, Ni-rich silicides

formed instead of NiSi at narrow gate lengths. This was mainly attributed to excessive Ni diffusion from areas surrounding the gates.

In the previous study, it was shown that although the annealing temperature was the most important control parameter in NiSi formation, the thickness of the as-deposited Ni layer and the reacted Ni-Si ratio can also influence, and sometimes dictate, phase formation in the silicide process. In the following part, NiSi nanolines were formed by reacting a Ni layer on top of Si nanolines, which was fabricated by using the fabrication process developed, and the linewidth effect on silicide formation was studied.

5.1.4 Linewidth effect on silicide formation

From the annealing profile in Figure 5.1(a), 420°C was selected as the annealing temperature for NiSi formation. Figure 5.5 shows a cross-sectional TEM image of a silicide line formation on a SOI wafer. It is noted that a thin layer formed on top of the buried oxide layer, due to the reaction between Ni and oxide in annealing. To suppress this lateral silicide growth [122], a two-step Ni-silicide process was used in the following annealing process to reduce the thermal budget of the first step annealing [17,123]. The first silicidation was chosen to be at 320°C for 1 minute. After selective removal of the unreacted nickel in the trench area, NiSi phase formation was conducted by a second step of annealing at 420°C. By comparing the sheet resistance of the NiSi layer that was formed after 2-step annealing with that formed by one-step annealing, it was confirmed that NiSi formation was achieved by the second annealing step.

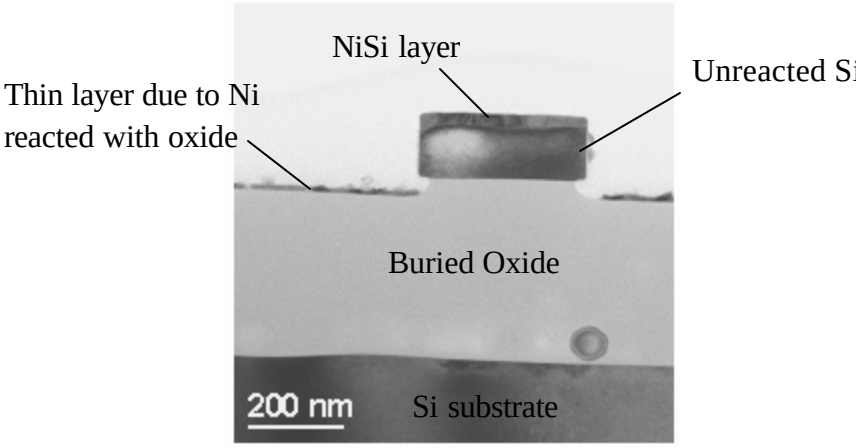


Figure 5.5 Cross sectional TEM image of a silicide line on SOI wafer after annealing at 420°C, showing a thin layer of NiSi formed on top of the unreacted Si nanolines. It is noted that there was a thin layer formed on top of the buried oxide, which was due to the reaction between Ni and oxide at 420°C.

In a following study of the linewidth effect, the silicon nanolines were fabricated on a (110) SOI wafer, with a 34 nm thick (110) silicon device layer and a 153 nm buried oxide layer. A ~ 8 nm Ni layer was evaporated on top of the nanolines, ensuring no influence from ultra-thin or excessive as-deposited Ni coating. Then the 2-step annealing process was applied to investigate the linewidth effect on NiSi formation in nanometric scale. Figure 5.6 shows a plan view SEM image of a set of silicon nanolines fabricated by EBL+AWE. The linewidths varied from ~15 nm to ~500 nm, with line height defined by the thickness of the device layer. Figure 5.7(a) shows a cross-sectional TEM image of the 500 nm wide silicide line, indicating a ~17 nm thick silicide layer formed on top of ~ 20 nm thick unreacted (110) silicon layer. The thickness of the silicide layer was the same as that of NiSi film formed on silicon substrate, which was 2.2 times the thickness of the as-

deposited Ni layer. Based on the HRTEM image of the interface area shown in Figure 5.7(b), and the corresponding two dimensional FFT image in Figure 5.7(c), the silicide layer was identified to be orthorhombic NiSi. The zone axis of $[2\bar{3}1]$ is parallel to Si zone axis of $[\bar{1}12]$. The sheet resistance of the formed NiSi film was measured to be 11.8 Ω/ , which corresponded to a resistivity of around 20 μΩ·cm. This value was slightly higher than that of NiSi film formed on the Si substrate, possibly due to the quality (*e.g.* defect level control) of the silicon device layer being not as good as the (110) silicon wafer.

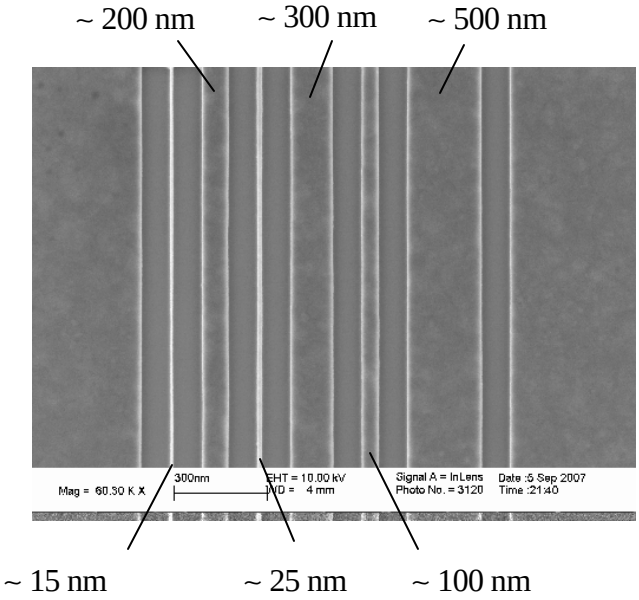


Figure 5.6 Plan view SEM image of a set of silicide nanolines after the annealing process. Linewidths varied from ~20 nm to ~500 nm, fabricated by the developed process on a (110) SOI wafer.

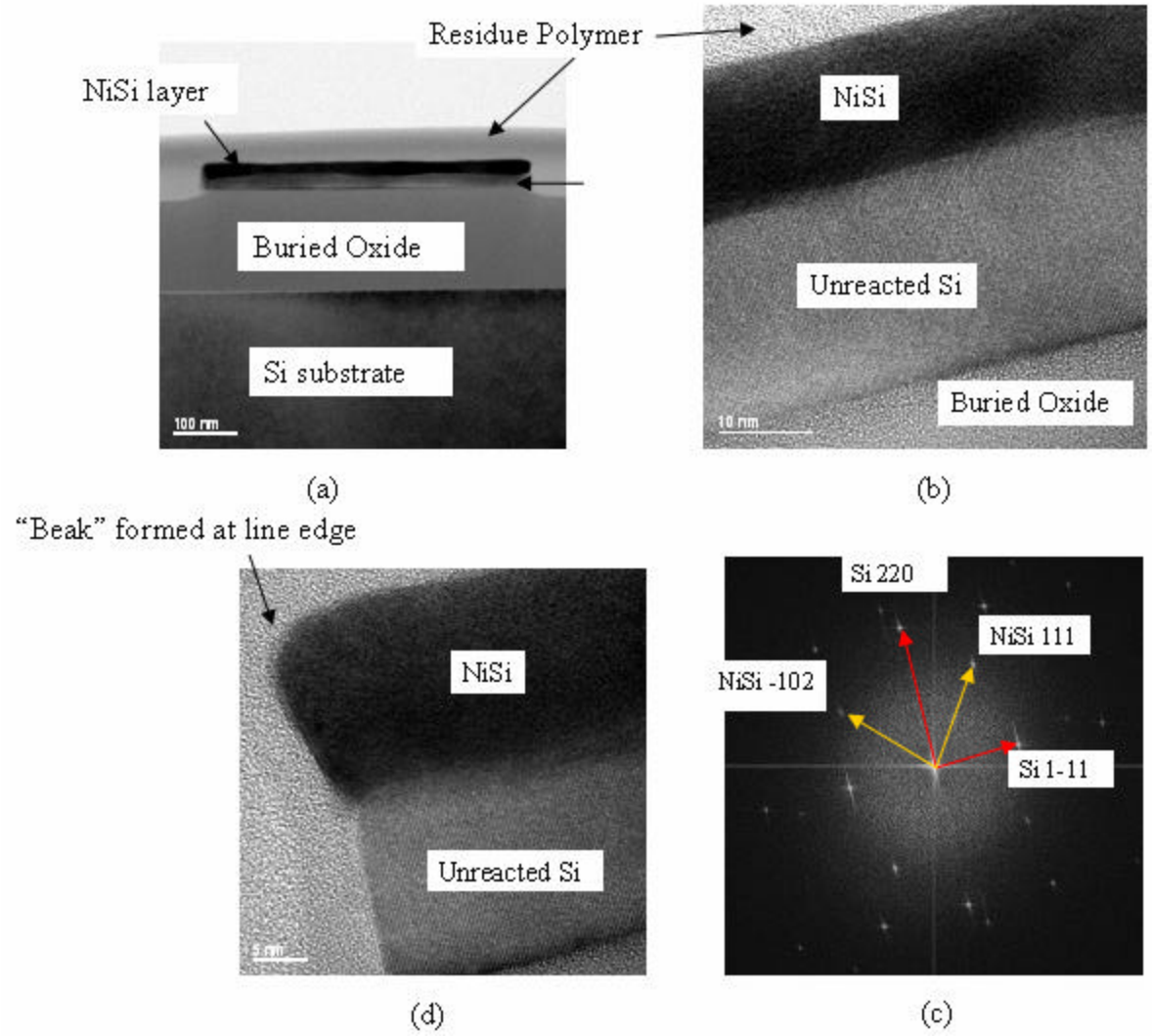


Figure 5.7 (a) Cross-sectional TEM image of the 500 nm silicide lines on SOI wafer, showing a ~17 nm silicide layer formed in (110) device layer. (b) HRTEM image around the interface area. The silicide layer is identified to be orthorhombic NiSi by the two dimensional Fourier transform of image in (c), depicting that NiSi zone axis $[2\bar{3}1]$ is parallel to Si zone axis $[\bar{1}12]$. (d) Cross-sectional HRTEM image of one edge of the line, showing excessive NiSi formation at line corner. This might result in the formation of a "beak"-like shape at line corner.

It is interesting to note that there was a "beak" shape formed at the line edge, which is shown in Figure 5.7(d). This feature might be caused by excessive Ni deposition on the line edge during the e-beam evaporation, resulting in the formation of an extrusion at the line corner after annealing. In the HRTEM image in Figure 5.8(a), it is shown that the cross-section of the narrowest silicide line was more like a trapezoidal shape than a rectangle, indicating an apparent corner effect in silicide formation. The effect of corner extrusion was obvious for the narrow silicide lines. The line width at half way point of line height was determined to be around 15 nm. The width of the underlying silicon line was a little narrower than that of the silicide layer on top, which was determined to be 13 nm. It indicates that the fabrication process developed could be used to form silicon lines with feature size close to ten nanometers. The thickness of the silicide layer was measured to be ~ 23 nm. From the TEM images, it is clear that narrow silicide nanolines (25 nm wide or below) were ~ 30% thicker than wide silicide line (200 nm or wider), which was ~17 nm thick as shown in Figure 5.7(a) and Figure 5.8(b). The observation of line edge effect is similar to that reported in reference [76], which showed that the thickness of 0.1 um wide NiSi line was greater at the line edge than at the center. The phenomenon was also attributed to excessive Ni diffusion from the surroundings at the edge areas. In this study for phase analysis, energy dispersive X-ray spectroscopy (EDS) measurements showed that the composition ratio of Ni to Si of the silicide layer in both 500 nm line and the 15 nm line were the same, confirming the formation of NiSi with the 2-step annealing process. The geometry difference between wide and fine silicide lines clearly indicated that, for the electron transport study in tens of nanometric level, it was

necessary to consider line geometry effect in silicide formation, because the resistivity results were directly related to details of the line profile.

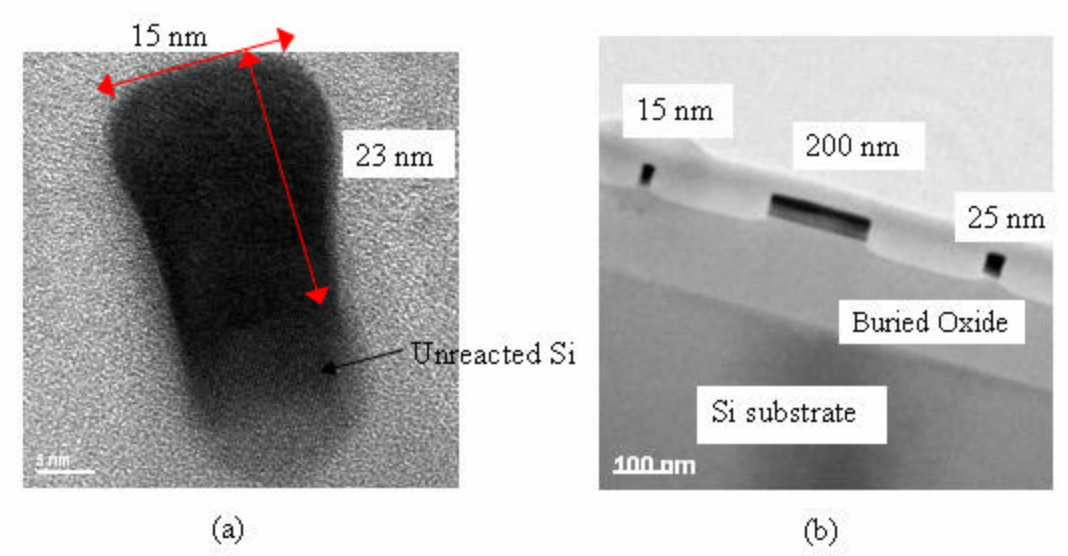


Figure 5.8 (a) HRTEM image of the 15 nm wide silicide line, showing a trapezoid-like silicide layer formed on top of the un-reacted (110) silicon; (b) Cross-sectional TEM image of a set of silicide lines on SOI wafer, showing silicide layer thickness on fine lines (25 nm line and 15 nm line) was larger than that on 200 nm wide lines.

5.2 Electron transport in NiSi nano-lines

In the electrical transport study in nickel silicide, it was necessary to form electrical test structures on top of (110) SOI wafer, including nanolines and the connected bond pads. The first part in the following section covers the design and fabrication of a four terminal probe test structures (Kelvin structure) with feature size down to 23 nm. The second part is about the resistivity measurement results at room temperature. The Fuchs-Sondheimer's (FS) surface scattering model was used to explain the resistivity results. To further investigate the sidewall scattering effect, resistivity measurements

were performed at low temperatures in a cryostat, which is presented in the third part. It is shown that the sidewall scattering effect on electron transport in silicide lines was observed only at low temperatures, because the electron mean free path of NiSi at room temperature is as small as ~ 5 nm.

5.2.1 Design and fabrication of electrical test structures

To fabricate ultra-fine nanolines, positive tone e-beam resist was used for better resolution compared with negative tone resist. In this case, to save e-beam writing time for large area probe pads in resistance measurement, a novel four terminal probe test structure was designed. The schematic is shown in Figure 5.9(a). The colored areas correspond to those of resist exposed to e-beam and are then removed by developer. The white areas are those where conductive silicide formed after the annealing process. Figure 5.9(b) shows a SEM image of a fabricated test structure with silicide grain size around 100 nm. The width of the separation trench to form bond pads was around 200 nm. In measurement, probe pads 1 and 2 were used to force current, and probe pads 3 and 4 were used to provide V/I measurements of silicide with line length around 5.5 μm. For consideration of wet etching along {111} planes, in Figure 5.9, the inner angle of the probe pad was 70.5°, which was the angle between two {111} crystalline planes in a cubic structure. Figure 5.10 shows two SEM images of the silicide nanoline test structures fabricated by wet etching and dry etching processes, respectively. It is clear that with the wet etching process, the NiSi nanoline fabricated in Figure 5.9(a) was straight, well defined, and much smoother than that by the dry etching process in Figure

5.10(b). The good quality of the nanolines fabricated by AWE process enabled precise measurement to be made on line cross-section profile in the resistivity tests.

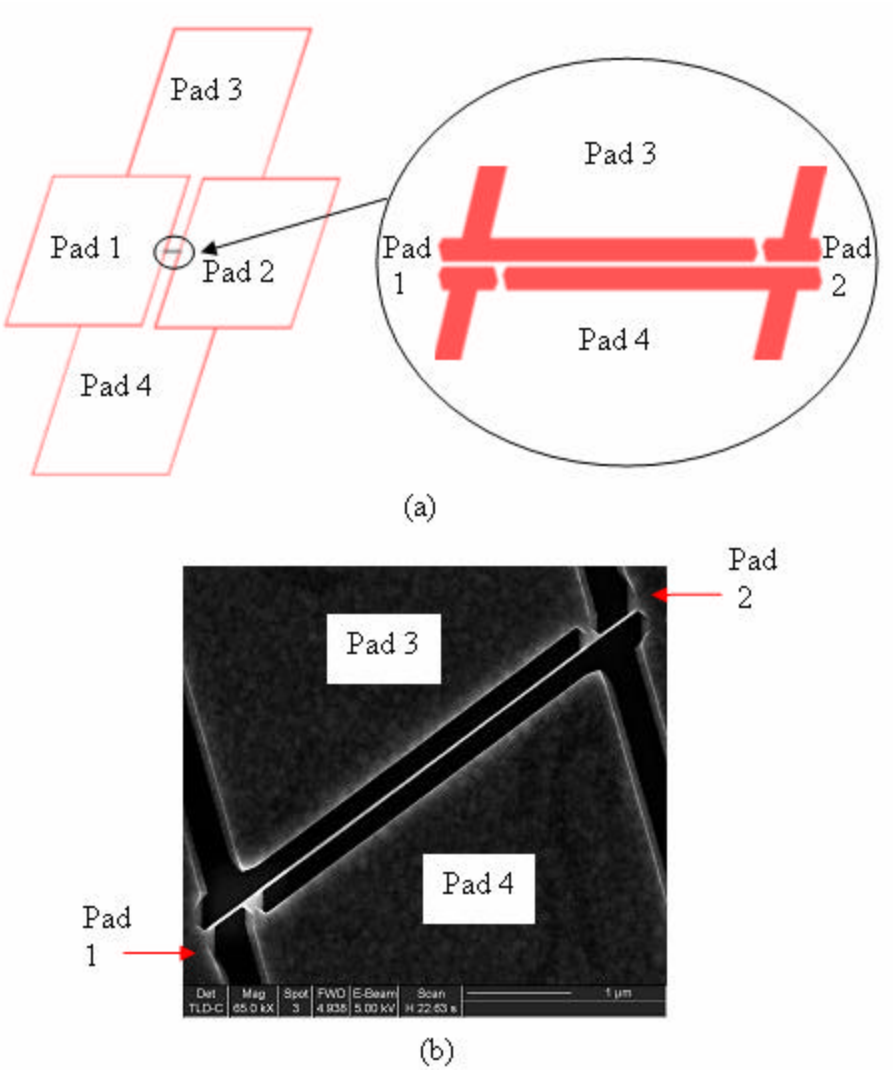


Figure 5.9 The four terminal probe test structure designed for resistance measurement on silicide fine lines. (a) Schematic of the test structure formed by e-beam lithography with a positive resist. The colored areas correspond to those of resist exposed to e-beam and are then removed by developer. The blank areas are those where conductive NiSi forms after annealing process. In the measurement, probe pads 1 and 2 were used to force current, and probe pads 3 and 4 were used to provide V/I measurements of line length around 5.5 μm. (b) SEM image of the test structure after silicide line formation. The width of the separation trench was around 200 nm and the grain size was around 100 nm.

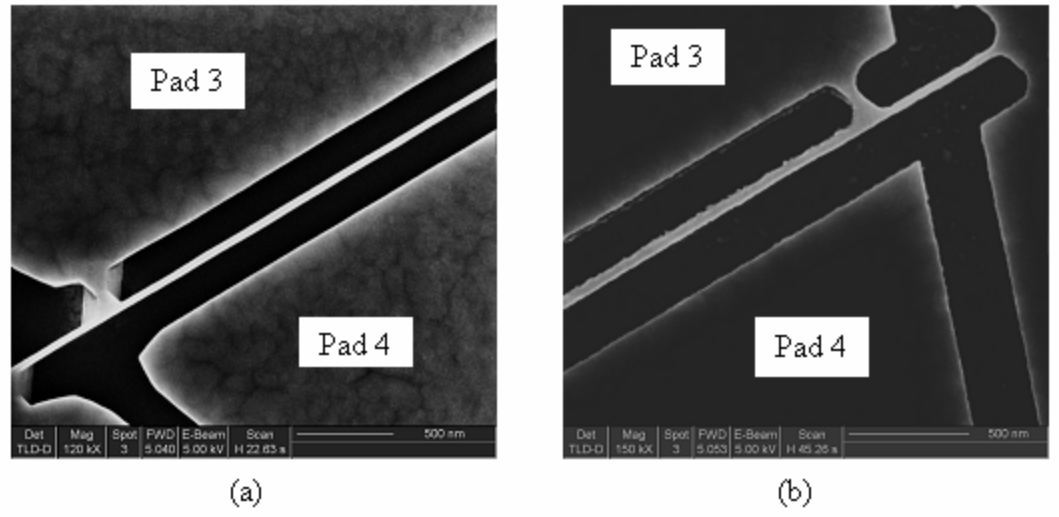


Figure 5.10 SEM images of NiSi test structures. (a) Pattern transfer using wet etching process; Lines are straight and well defined; (b) Pattern transfer using drying etching process, showing roughness at line edges.

5.2.2 Resistivity measurements at room temperature

To investigate scaling effect on the NiSi resistivity, two silicide test structures with nominal widths of 30 nm and 460 nm were fabricated on a (110) SOI wafer. The (110) silicon device layer was ~ 60 nm thick. The thickness of the as-deposited Ni was 12 nm thick and the sample was subjected to the same 2-step annealing process. The nanoline geometry of the fine line was determined by cross-sectional HRTEM imaging. Figure 5.11 shows the TEM images of the cross section of the ~ 23 nm nanoline, indicating a crystalline silicide layer forming on top of the un-reacted silicon layer. The nanoline was ~31 nm thick, showing a familiar trapezoidal shape cross-section. For features with a nominal width of 460 nm, the linewidth was measured by SEM imaging and found to be about 455 nm. The height of the line was measured, by HRTEM imaging,

to be ~ 27 nm, which was also the thickness of the silicide film. The silicide phase was found to be nickel mono-silicide based on micro-structural analysis in section 5.1.4, because the same annealing process was applied in the silicide formation.

For Kelvin resistance measurements, probe pads 1 and 2 were used for applying current and probe pads 3 and 4 were used for voltage sensing, which is shown in Figure 5.9. The I-V curves showed a linear behavior as shown in Figure 5.12. The resistances of the nanolines were determined by the slopes of the curves. The current leakage through the separation trench and through the intrinsic un-reacted silicon layer was negligible, according to the experiments performed. The measured resistivities of the silicide lines at room temperature are summarized in Table 5.1.

Table 5.1 The measured resistivity of NiSi nanolines at room temperature for two set of test structures with different line widths. The measured line length is around 5.5 μm.

	Measured linewidth (nm)	Measured thickness (nm)	Measured line resistance (Ω)	Effective Resistivity (μΩcm)
NiSi fine lines made by wet etching	455	27	66.4	19.7
	23	31	1136.0	19.5

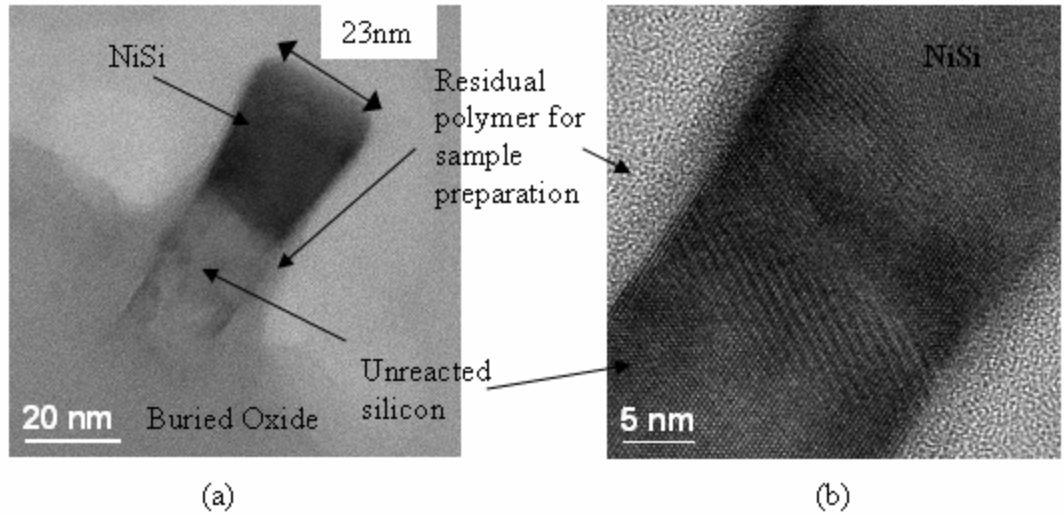


Figure 5.11 Cross-sectional TEM images of NiSi test fine line. (a) Overview; linewidth and line height were determined to be 23 nm and 31 nm, respectively; (b) HRTEM image around interface area, showing NiSi crystalline structure formed on top of the unreacted Si.

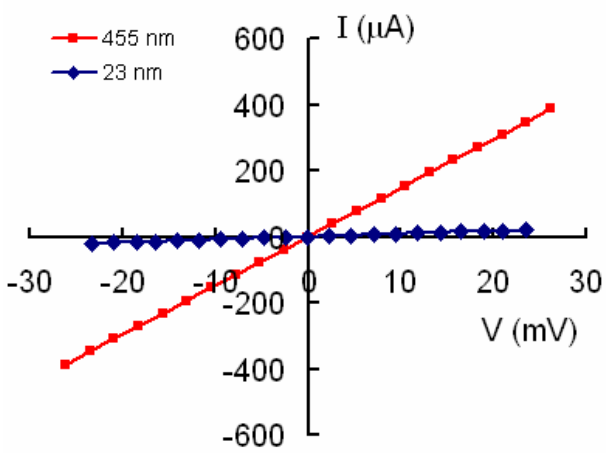


Figure 5.12 Current vs. voltage curves of the resistance measurements on 455 nm and 23 nm wide NiSi nanolines. The relationship was linear and resistance was determined from slopes for the two curves.

The measured resistivities for both line widths were around 20 μΩ-Cm at room temperature, which was in good agreement with published measurements [73,76,119] and the measurements we conducted on nickel silicide films. From the linewidth independency, it was concluded that side wall scattering did not reduce the mean free path at room temperature. This observation can be attributed to the small mean free path for electron scattering in bulk nickel monosilicide, which is approximately 5 nm at room temperature [119,124]. For a simple estimation of the influence of sidewall scattering, the thickness dependent resistivity of nickel silicide film was calculated according to the well-known Fuchs-Sondheimer's (FS) surface scattering model [69,70]. Hence, the resistivity of thin films is given by:

$$\frac{r_s}{r_0} = \left[1 - \left(\frac{3}{2k}\right)(1-p)\int_1^{\infty}\left(\frac{1}{t^3} - \frac{1}{t^5}\right)\frac{1-e^{-kt}}{1-pe^{-kt}}dt\right]^{-1} \tag{5.1}$$

where ρ_s is the resistivity of the thin film, ρ_0 is the bulk resistivity, κ is the ratio of the film thickness to the bulk mean free path, p is the probability that an electron will be specularly reflected from a film surface (p=0, inelastic and diffusive scattering at interface). Figure 5.13 shows the calculated ρ_s/ρ_0 curve of NiSi film at various thicknesses. The electron mean free path at room temperature of NiSi was set to be 5 nm in this model. It is shown that as film thickness scaled down to 23 nm, the maximum resistivity change of film over bulk materials was only around 9%, for p=0 and totally inelastic or diffusive electron scattering. The results from our measurements and the FS model suggested that due to the inherent effect of small electron mean free path [125], there was no significant width effect as feature size scaled down to 23 nm, assuming

grain boundary scattering was not dominant due to a large grain size ~ 100 nm as estimated in Figure 5.9.

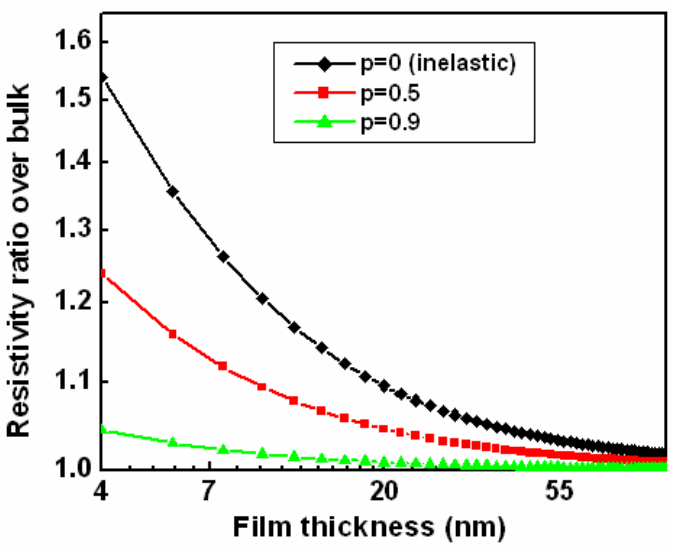


Figure 5.13 Plot of Equation (1). The resistivity ratio over bulk (ρ_s/ρ_0) vs. film thickness. p is the probability that an electron specularly reflected from surfaces.

5.2.3 Low temperature resistivity measurement

To further investigate the scaling effect on electron transport in nickel silicide lines, low temperature resistance measurements were performed in a cryostat chamber with temperature down to 7K. Based on Matthiessen's rule,

$$r = r_r + r(T) \tag{5.2}$$

The resistivity of silicide lines is the sum of the residual resistivity ρ_r and the temperature-dependent resistivity $\rho(T)$. Here, ρ_r includes the contribution of scattering from sidewalls, surface, grain boundary, defect and impurity, and $\rho(T)$ is caused by electron-phonon scattering and temperature dependent.

For ρ(T), according to Bloch-Gruneisen (BG) relation:

$$r(T) = 4(\frac{T}{q_D})^5 r_q \int_0^{q_D/T} \frac{x^5 e^x}{(e^x - 1)^2} dx \qquad (5.3)$$

where θ_D is Debye temperature, which is around 500K for NiSi [126]. ρ_θ is the prefactor of the BG equation. At high temperatures ranging from $T>0.2\theta_D$, the relationship between resistivity and temperature could be reduced to a linear relation:

$$\rho(T) = \rho_0 [1 + a(T - T_0)] \qquad (5.4)$$

where a is the temperature coefficient of resistance measured at temperature T_0. At the low temperature range, ρ(T) is proportional to T^5 and will vanishes as $T \to 0$. Since the electron mean free path λ is

$$l = \frac{h(3/8p)^{1/3}}{e^2 r n^{2/3}} \qquad (5.5)$$

where n is carrier density, which does not change significantly in metals as temperature decreases. Thus the formula can be rewritten as:

$$l r = \frac{h(3/8p)^{1/3}}{e^2 n^{2/3}} \approx Const. \qquad (5.6)$$

The equations indicate that as the resistivity of metal decreases with temperature due to weaker electron-phonon scattering, the electron mean free path increases accordingly. Figure 5.14 shows the resistivity of nickel silicide vs. temperature in a range of 7-300K. The measured resistivities for both silicide wide and narrow line structures were similar in the high temperature range, *i.e.* T>100K, suggesting no significant sidewall scattering effect on electron transport. The residual effective resistivity of 23 nm wide line, 6.3 μΩ·cm, was about 26% larger than that of 455 nm wide line of 4.6 μΩ·Cm, indicating the size effect of electron scattering when mean free path increased to be comparable with the line width. The increase of residual resistivity at cryogenic temperature in the fine

line had two origins: one was that the sidewall scattering of electron due to the fine line was narrower than the wide line, and another may be come from the grain boundary scattering because the grain size of fine line may be smaller than that of wide line.

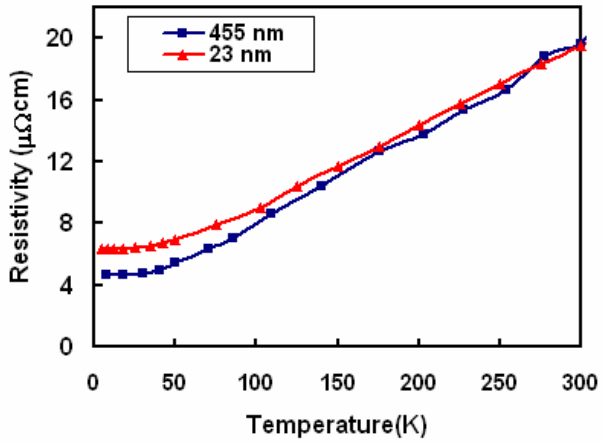


Figure 5.14 Resistivity of NiSi lines in temperature ranging from 7-300K. The residual resistivity of 23 nm wide line was higher than that of 455 nm wide line, indicating the effect of sidewall scattering as electron mean free path increased to be comparable with line width at low temperature.

According to Eqs. 5.6 and assuming that the electron mean free path λ of NiSi is 5 nm at room temperature, the λ vs. temperature curves could be calculated as shown in Figure 5.15. It shows that as temperature reduced to below 100K and the λ increased to beyond ~ 11 nm, the sidewall scattering effect on electron transport in 23 nm line became obvious. As the temperature reduced to as low as 7K, assuming that the scattering mechanisms are independent of each other, we have:

$$1/\lambda_{455\,nm} = 1/\lambda_{electron\text{-}phonon}(T) + 1/\lambda_{defects} + 1/\lambda_{top\text{-}bottom\ surfaces} \quad (5.7)$$

$$1/\lambda_{23nm} = 1/\lambda_{electron\text{-}phonon}(T) + 1/\lambda_{defects} + 1/\lambda_{top\text{-}bottom\ surfaces} + 1/\lambda_{sidewalls} \quad (5.8)$$

where $1/\lambda_{455nm}$ and $1/\lambda_{23nm}$ represent the total scattering of electron transport in 455 nm and 23 nm wide nanolines, respectively. $1/\lambda_{defects}$ and $1/\lambda_{sidewalls}$ represent defect scattering and sidewall scattering, respectively. $1/\lambda_{top\text{-}bottom\ surfaces}$ resembles the electron scattering from the top and bottom surfaces of the NiSi layer. Assume the defect scattering and top-bottom surface scattering in 455 nm and 23 nm wide lines are similar, then the sidewall scattering effect can be roughly estimated by subtracting Eqs.5.8 to Eqs. 5.7:

$$\lambda_{sidewalls} \approx \frac{1}{1/l_{23nm} - 1/l_{455nm}} \approx 63\ \text{nm} \tag{5.9}$$

Thus the specularity of electron scattered at the sidewalls is estimated to be

$$p \approx 1-\lambda_{23nm}/\lambda_{sidewalls} \approx 0.7 \tag{5.10}$$

As a comparison, the specularity p is close to 0 for the surface scattering in copper interconnects [127,128]. This indicates that sidewall surface roughness of the 23 nm NiSi lines are smaller than that of copper interconnects.

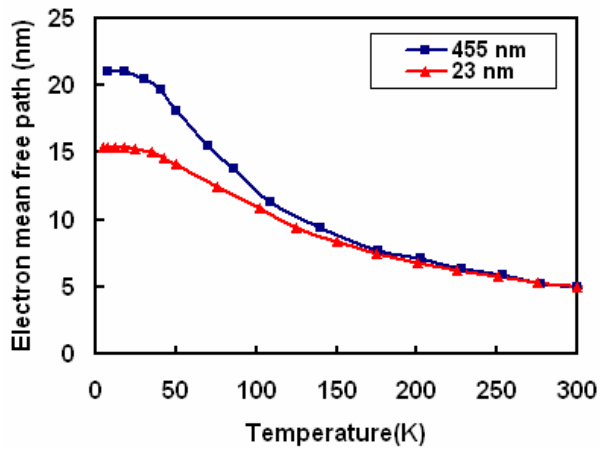


Figure 5.15 The estimated electron mean free path vs. Temperature curves for the silicide nanolines. Assume λ is 5 nm at room temperature and $\rho\lambda \approx$ constant as temperature changes.

It should be noted that this was only a rough estimation. For a precise calculation, Low temperature Hall measurement needs to be performed in a high magnetic field to evaluate carrier density in NiSi at various temperatures.

5.3 Summary

In the nickel silicide formation study, Ni layer was evaporated on Si wafers and then subjected to an annealing process for silicide formation. It turned out that besides the annealing temperature, the as-deposited Ni thickness and the reacted Ni-Si ratio also influenced the formation of NiSi. With a 10 nm Ni coating, low resistivity NiSi was formed in the temperature window from 300°C to 550°C. For ultra-thin Ni coatings, *i.e.* 2.5 nm thick Ni coating, the $NiSi_2$ phase and a coherent interface were formed in this temperature window. However, if excessive Ni existed in the Ni-Si reaction, Ni-rich phase such as Ni_2Si was formed even at a temperature as high as 550°C.

In a subsequent study, silicon-based nano-structures with vertical and smooth side walls were fabricated using AWE on SOI wafers with (110) orientation. Nickel silicide lines with feature size down to 15 nm were formed by annealing the nickel coating deposited on the single-crystal silicon fine line structures. Using HRTEM technique, it is shown that, for 25 nm wide fine lines and below, the cross sections of silicide lines were affected by the corner extrusion effect, resulting in formation of a trapezoidal profile and a thicker NiSi layer. This was due to an excessive Ni deposition on line edges during the e-beam evaporation. Such behavior suggests that it would be necessary to consider line geometry effect in tens of nanometer scale. The four-probe electrical measurements at

room temperature revealed little resistivity difference between the 455 nm wide line and the 23 nm wide line. This is consistent with the fact that the bulk mean free path for electron scattering in nickel monosilicide is much smaller than the linewidth dimensions in this study. The measured residual resistivity at cryogenic temperature increased with decreasing line width, suggesting decreased electron mean free path of sidewall scattering with decreasing linewidth.

Chapter 6 Summary and Future Work

6.1 Summary

With the integrated circuit dimension scaling continuing beyond the 65 nm node, the fabrication of nanoscale structures and the evaluation of their material properties became a big challenge for future development of the interconnect technology. The size-scale effect can modify material properties and make them quite different from its bulk value. It is important to investigate the scaling effect on material properties for both scientific understanding and for industrial applications. This research focused on fabrication and characterization of material properties of small-dimension silicon-based structures, which includes three parts: fabrication process development for silicon nano-structures, mechanical characterization of patterned silicon nano-lines, and electron transport study in nickel silicide fine lines.

In this study, a top-down fabrication process was developed, which combined electron-beam lithography (EBL) and anisotropic wet etching, to obtain single-crystal, parallel Si nanolines (SiNLs) on a (110) Si wafer or (110) silicon layer on a SOI wafer. The fabrication began with a thin chromium layer deposited on a Si (110) wafer which was covered with an oxide layer by chemical vapor deposition. After the chromium coating, a positive resist was spun on the wafer and then imaged using an electron-beam exposure system. The chromium layer was used as a hard mask for patterning the oxide layer by a reactive ion etching (RIE) process. The oxide layer in turn served as an etching mask for pattern transfer to silicon by etching using tetra-methyl-ammonium hydroxide (TMAH). With plasma etching, the pattern was first transferred from the resist layer to

the chromium lines. Subsequently, the residual resist was removed and TMAH was used for anisotropic etching of the Si along {111} crystalline planes. When the openings were aligned with one of the <112> directions, vertical and nearly atomically flat sidewalls were formed along the {111} orientation. Finally, the chromium and oxide hard masks were removed by chromium etchant and buffered oxide etchant, respectively. Using the same approach, SiNLs with line widths as small as 25 nm were successfully fabricated. A line width as small as 12 nm is achievable. The height of the SiNLs could be controlled by TMAH etching time within the range of 200nm to 1500 nm. The good crystal quality and well-defined geometry, along with the smooth sidewalls and the highly uniform line width, make these SiNLs well suited for accurate experimental measurements as well as numerical modeling.

In the mechanical characterization, an AFM based nanoindentation system was employed, and the elastic, fracture, and frictional properties of three sets of Si nanolines were characterized. The SiNLs had the linewidth ranging from 24 nm to 90 nm, and the aspect ratio (Height/linewidth) from 7 to 18. The elastic modulus of the SiNLs was found to be similar to its bulk, showing an insensitivity of modulus to the scaling effect. A buckling instability was observed at a critical load, with fully recoverable deformation after withdrawal of the indenter. A finite element model (FEM) was developed to simulate the elastic response, to predict the critical load, and to determine the magnitude of the displacement burst. It was found the deformation behavior of the SiNLs depended on the combined effects of load, line geometry, and the friction at contact. Friction properties at nanoscale were characterized, with friction coefficient ranging from 0.01 to

0.05. These values were much smaller than the friction coefficient in macro scale (> 0.1), showing localized contact area at nanoscale. Meanwhile, the friction properties at the contact played an important role in controlling buckling mode of SiNLs. For experiments with larger indentation displacements, irrecoverable indentation displacements were observed due to fracture of Si nanolines, with the strain to failure estimated to be from 3.8% to 9.7%. This study demonstrated a valuable approach to fabrication of well-defined Si nanoline structures and the application of the nanoindentation method for investigation their mechanical properties in the nanoscale.

In the electron transport study, a set of silicon nanolines with feature sizes down to 12 nm was fabricated using the process developed for (110) SOI wafers, in which the buried oxide layer served as an etch stop layer for TMAH etching. Ni was deposited on these nanolines, and then annealed to produce nickel silicide nanowires. The linewidth effect on nickel silicide formation was studied using high-resolution transmission electron microscopy (HRTEM). It was shown that as linewidth reduced below 25nm the silicide layer became thicker than that formed on wider lines. This may be attributed to deposition of excessive Ni on line edges during evaporation, suggesting the necessity of considering the line geometry effect in silicide formation in tens of nanometer scale. Kelvin electrical measurements showed that the residual effective resistivity of the silicide lines at cryogenic temperature increased with decreasing line width, indicating an increase of electron surface scattering with decreasing line width. A mean free path for electron transport at room temperature of 5 nm was deduced, which suggests that nickel silicide can be used without degradation of device performance in nanoscale electronics.

6.2 Recommendations for future work

A scaling effect study requires us to fabricate nano-structures as small as possible. However, the process control on fabrication of high quality nano-structures is very challenging, particularly for the formation of ultra-fine structures. As an extension of the current fabrication process, three possible methods to form nano-structures with CD down to 10 nm range could be considered:

1) Direct use of nano-lithography to define feature size to be as small as 10 nm. First this method requires a precise dose level in e-beam lithography as well as a precise etching rate in TMAH etching, since over-exposure or over-etching will cause such a fine line to easily break. Secondly, a careful orientation alignment is necessary, *e.g.* increasing the direction changing steps or decreasing the line length in the test pattern design.

2) Fabricate fine line at first, for example, SiNLs with CD around 20-30 nm. Then oxidize the surface of SiNLs by LPCVD and then use HF to remove the formed silicon oxide to further shrink linewidth. There are two considerations in this method. One is the influence of the thermal stress induced during oxidation process, since the process temperature normally is higher than 850°C. Another is the difficult formation of SiNLs on SOI wafers, because the removal of oxide may lift-off the ultra-fine lines.

3) Modify the process according to the fabrication methods reported in reference [129]. For example, form SiNLs on SOI wafer at first, and then oxidize or nitridize the surface of nanolines. Secondly, use RIE to remove oxide or nitride on top of SiNLs, then use silicon etchant to etch away silicon nanolines and leave oxide or nitride on top of the

buried oxide. In this method, linewidth is determined by thickness control of thin film formed at sidewall of SiNLs. Instead of oxidizing or nitridizing surface, use of e-beam evaporation or sputtering to coat a metal layer (*e.g.* Al, Cr, etc) on the sidewall may enable the formation of ultra-fine metal lines.

Characterization of ultra-fine nanostructures is also very challenging. Generally speaking, because process control becomes more difficult for smaller structures, the measurement results are expected to be subjected to large data scattering accordingly. One strategy is to determine collective responses of multiple nano-structures to mitigate this influence.

Since surface to volume ratio keeps increasing as line width decreases, the surface characteristics become increasingly important in determining the mechanical or electrical properties of nanostructures. For example, as the linewidth scaled to the 10 nm range, change of elastic modulus may be expected, because the atomic bonding status at the surface is quite different from that of the interior. Until now, no experimental data has been reported at such a small scale, and the metrology used in this dissertation should enable these mechanical measurements to be performed.

Besides an investigation of elastic modulus of ultra-fine nano-structures, the scaling effect on fracture strength is also an important topic. It is known that the theoretical limit of strain to failure of silicon is close to 17%. Hence the investigation of silicon strength under an ultra-small scale is of great importance for scientific understanding of facture of nanostructures. Meanwhile, if ultra-fine metal lines could be fabricated, the indentation measurement on these metal lines will open windows to

understand deformation mechanism of metal at the nanometer scale. Again, the measurement would not be easy to perform due to the stringent requirement on fabrication and measurement control.

The friction property at nanoscale is of fundamental interest. The indentation measurement on SiNLs provides a valuable metrology for characterizing friction at the contact between indenter and nanoscale silicon. There are two possible methods to change friction coefficient at the contact: one is to oxidize or nitridize the surface of SiNLs, or coat a thin metal layer on SiNLs; another is to change the indenter material, *e.g.* use tungsten carbide indenter instead of diamond indenter. It would be of great interest to investigate the corresponding change of mechanical responses due to the change of the friction coefficient.

Another interesting topic is investigation of the influence of surface defects on indentation responses. For example, slightly oxidize surface of SiNLs and then use HF to etch off the formed oxide, may further polish surface of nanoline and improve its quality. This polishing process may affect fracture strength and friction properties of SiNLs. Nanoindentation tests before and after the polishing would help us to understand this effect.

For metrology, one of the big concerns in the mechanical tests is the resolution and sensitivity requirement for the force transducer. The noise level of the current indentation system was ~ 1 μN, thus the peak load applied had to be larger than 10 μN to avoid noise influence. Since fine lines are weaker than wide lines, two strategies are useful in the mechanical tests: one is to use large indenter or flat punch to sense

mechanical response of multiple nanolines, and another is to reduce the aspect ratio (height/width) of fine lines to increase their bending stiffness.

FEM simulation is very useful to extract material properties and to understand buckling behavior of nanolines. The current model could be used to analyze elastic responses in loading, and could predict buckling instability at a critical load. However, it is still a simple model and needs to be upgraded for better interpretation of indentation results. Some key improvements are needed, including a) dealing with divergence issue during the FEM calculation; b) post-buckling analysis, for example, to understand displacement burst in the unloading, load vs. displacement curve hysteresis, etc. c) dynamic loading-unloading effect on the indentation responses. d) validity of the assumption of rigid substrate on the extraction of maximum bending strain in SiNLs. All these issues need to be addressed by refining the model.

In the electrical study, it turns out that carrier density is an important parameter for precise characterization of scattering mechanisms. The determination of carrier density needs a Hall-effect measurement. Meanwhile, in order to observe the sidewall scattering effect at room temperature, it would be interesting to perform resistance measurements on NiSi fine lines with the linewidth scaled down to several nanometer range. The microstructural analysis using TEM imaging should be developed even if it is very challenging at this scale. Since sample preparation is difficult, plus the volume being analyzed is quite small, it might be useful to measure multi-lines as an alternative.

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